MPC860DB & MPC860SARDB & MPC860TDB

Revision PILOT

User's Manual

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1 - General Information

1•1 Introduction

This document is the operation guide for the MPC8XXFADS Daughter Board which can be for MPC860T, MPC860SAR or MPC860- named the MPC860DB.

The daughter board holds The device (MPC860T or MPC860SAR or the MPC860) along with some necessary logic, which is required to be in the nearest vicinity of The device as well as peripherals, that are dedicated to the MPC860T and are not required for any other member of the MPC8XX family.

The daughter board has 2 sets of matching connectors - on the print[A] side and on the component[B] side. Those on the print side, connect to a matching set found on the MPC8XXFADS while those on the component side, are to serve hardware expansion via a dedicated adaptor.

In addition, a set of logic analyzer connectors is featured matching the new high density HP16500 logic analyzer adaptors, this to provide fast connection to logic analyzer while saving on board's space and reducing EMI.

1•2 Abbreviations' List

- FADS[C] - the MPC8XXFADS, to which this board connects.
- UPM - User Programmable Machine
- GPCM - General Purpose Chip-select Machine
- GPL - General Purpose Line (associated with the UPM)
- DB - Daughter Board the MPC860DB, the subject of this document.
- BSCR - Board Control & Status Register.
- ZIF - Zero Input Force
- BGA - Ball Grid Array
- Spec - engineering Specification Document.
- MPC - In this document it can be one of the MPC860T or MPC860SAR or MPC860.

1•3 Related Documentation

- MPC User's Manual.
- ADI Board Specification.
- MPC8XXFADS Engineering Specification
- Level One's LXT970 Data Sheet. May be obtained from http://www.level1/ds/970.html Relevant only for MPC860T
- MPC860SAR-PHY Board User Manual. Relevant only for MPC860SAR.

A. Board's bottom.
B. Board's top.
C. Not to be mistaken for the M683XX Family Ads

1•4 SPECIFICATIONS

The MPC860DB specifications are given in TABLE 1-1.

TABLE 1-1. 860DB Specifications

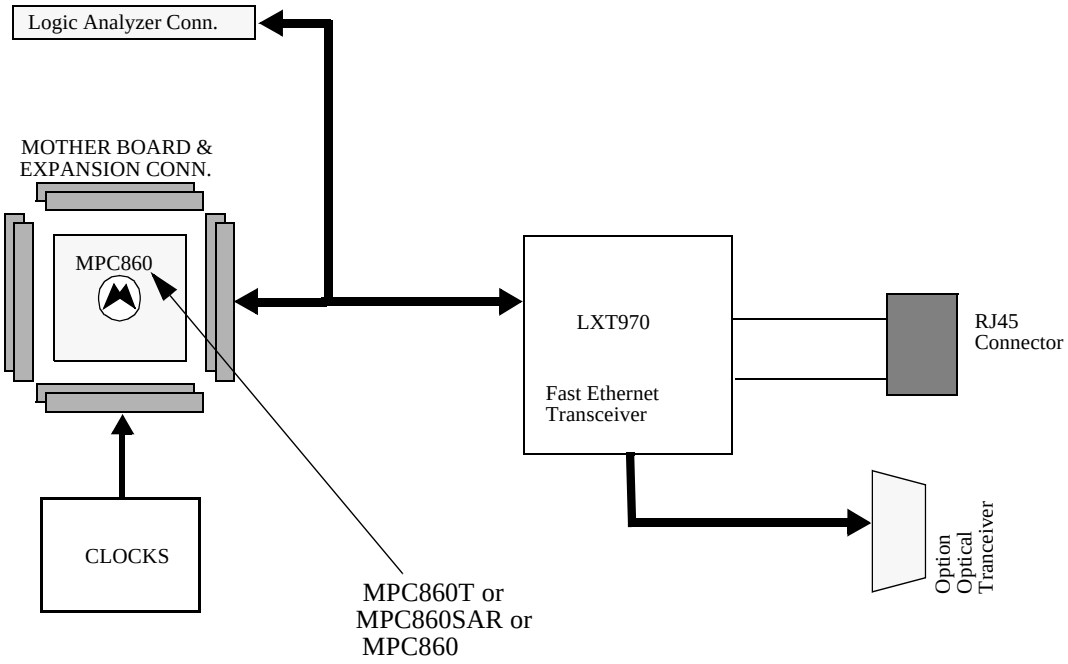
CHARACTERISTICS	*SPECIFICATIONS*
Microprocessor	MPC860T or MPC860SAR or the MPC860 @ 50 MHz
Operating temperature	0^{O}C - 30^{O}C
Storage temperature	-25^{O}C to 85^{O}C
Relative humidity	5% to 90% (non-condensing)
Dimensions: Length Width Thickness	145mm 125 mm 0.063" (1.6 mm)

1•5 MPC860DB Features

- MPC running upto 50 MHz
- On-Board Fast Ethernet Level One LXT970, with shutdown option over Twisted pair (Ethernet 100Base TX). (this device is only for MPC860T and it can be disabled).
- 5 Dip Switches for the LXT970 power up configuration.
- Option, for Fast Ethernet over Fiber Optics (Ethernet 100Base FX with MPC860T only).
- Selectable KAPWR source: 3.3V or externally supplied
- Selectable VDDL source: 3.3V or 2V
- Selectable clock source: 32768Hz crystal resonator or 4[A] MHz Clock generator.
- On-Board Expansion connectors, including all MPC pins and MPC8XXFADS control / status signals.
- On-Board High Density Logic Analyzer connectors, supporting fast connection to HP 16500 logic analyzer (AMP Mictor).

A. May be easily changed to any 3.3V powered oscillator oscillating in 3 - 5 MHz frequency range.

FIGURE 1-1 MPC860DB Block Diagram



2 - Hardware Preparation and Installation

2•1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the MPC860DB.

2•2 UNPACKING INSTRUCTIONS

NOTE

If the shipping carton is damaged upon receipt, request carrier's agent to be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

CAUTION

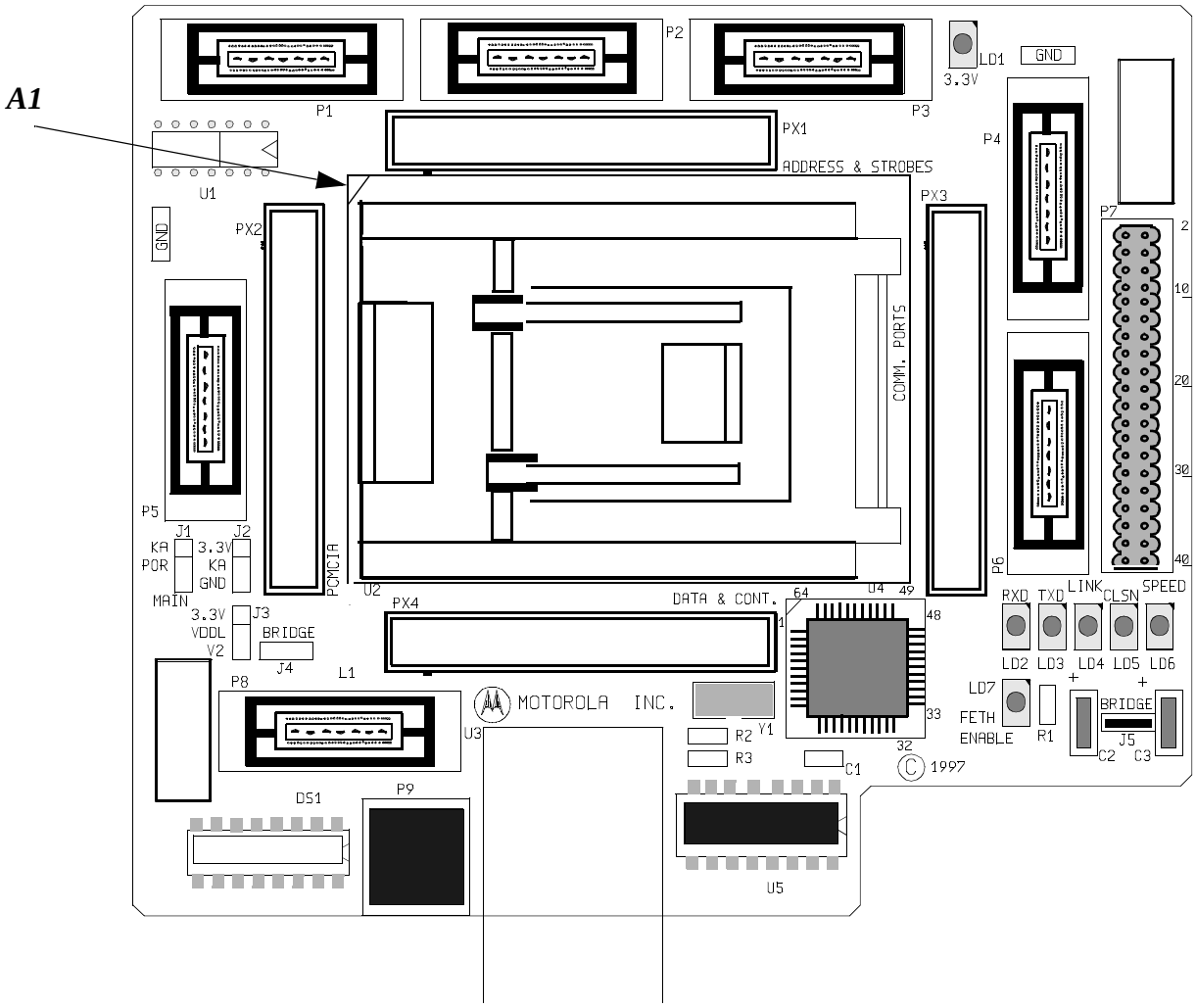
AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE CIRCUITS.

2•3 HARDWARE PREPARATION

To select the desired configuration and ensure proper operation of the MPC860DB board, changes of the jumpers settings may be required before installation. The location of the switches, LEDs, and connectors is illustrated in FIGURE 2-1 "MPC860DB Top Side Part Location diagram" on page 10. The board has been factory tested and is shipped with Dip-Switch settings as described in the following paragraphs. Parameters can be changed for the following conditions:

- Clock generator.
- Power-On Reset Source.
- MPC Keep Alive Power Source
- MPC Internal Logic Supply Source
- LXT970 power up configuration.

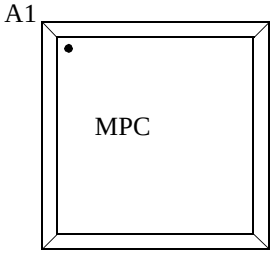
FIGURE 2-1 MPC860DB Top Side Part Location diagram



2•3•1 MPCs' Replacing - U2

Before replacing the MPC the user should turn off the power. When replacing U2 with another MPC it should be noticed where is the MPCs' A1 pin. Put the new MPC in the same direction as the old one.

2•3•1•1 MPC TOP VIEW

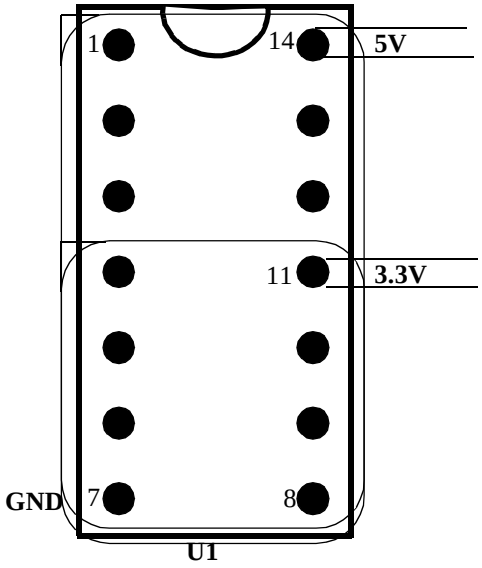


2•3•2 Clock Generator Replacement - U1

When replacing U1 with another clock generator it should be noticed that there are 2 supply level available at U1:

1) 5V supply at pin 14.
2) 3.3V supply available at pin 11.

FIGURE 2-2 U1 Power Sources



From looking at FIGURE 2-2 "U1 Power Sources" above, we see that 5V (with 3.3V output only!) oscillator may be used with 14 pins only form-factor while 3.3V oscillators may be used with 8 pins only form-factor.

WARNING

IF A 14 Pin Form-Factor, 3.3V Clock Generator is inserted to U1, PERMANENT DAMAGE Might Be Inflicted To The Device.

WARNING

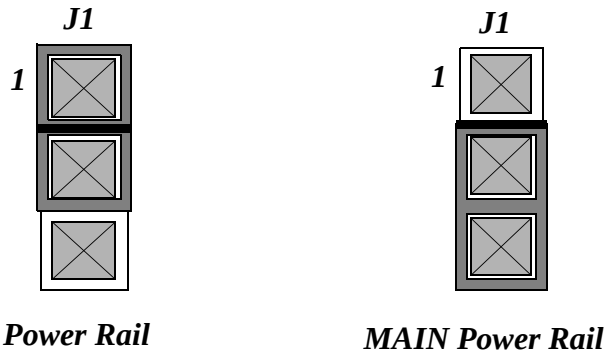
Since the MPC clock input is NOT 5V TOLERANT, any clock generator inserted to U1, MUST HAVE 3.3V compatible output. If a 5V output clock generator is inserted to U1, PERMANENT DAMAGE might be inflicted to the MPC.

2•3•3 Power-On Reset Source Selection

As there are differences between MPC revisions regarding the functionality of the Power-On Reset logic, it is therefore necessary to select different sources for Power-ON reset generation.

J1 on the MPC860DB is used to select Power-On Reset source: when a jumper is placed between positions 1 - 2 of J1, Power-On reset to the MPC is generated by the Keep-Alive power rail. I.e., When KAPWR goes below 2.005V - Power-On reset is generated. When a jumper is place between position 2 - 3 of J1, Power-On reset to the MPC is generated from the MAIN 3.3V power rail. I.e, when the MAIN 3.3V power rail goes below 2.805V Power-On reset is generated.

FIGURE 2-3 Power-On Reset Source Selection

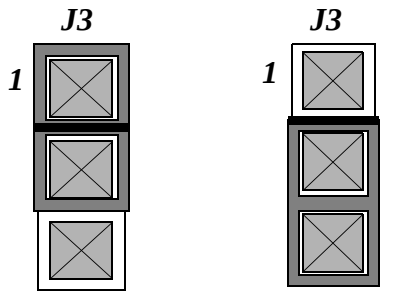


KA Power Rail *MAIN Power Rail*

2•3•4 VDDL Source Selection

J3 serves as a selector for VDDL - MPC internal logic supply. When a jumper is placed between positions 1 - 2 of J3, VDDL is supplied with 3.3V. When a jumper is placed between positions 2 - 3 of J3, VDDL is supplied by 2V power source. The jumper on J3 is factory set between positions 1 - 2 to supply 3.3 to VDDL.

FIGURE 2-4 VDDL Source Selection



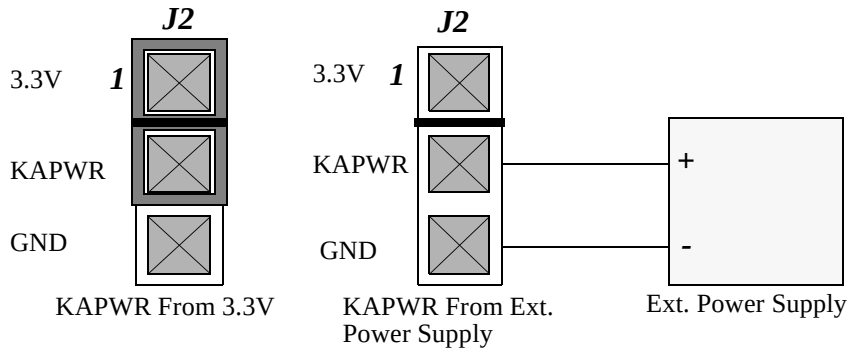
VDDL - 3.3V *VDDL - 2V*

2•3•5 Keep Alive Power Source Selection

J2 selects the Keep Alive power source of the MPC. When a jumper is placed between positions 1 - 2 of J2, the Keep Alive power is fed from the main 3.3V bus. When an external power source[A] is to be connected to the Keep Alive power rail, it should be connected between positions 2 (the positive pole) and position 3 (GND) of J2.

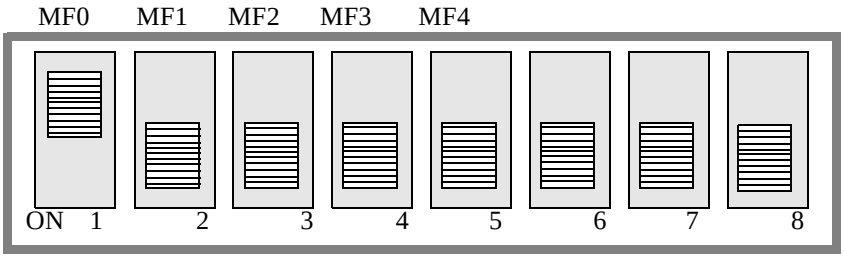
A. E.g., a battery.

FIGURE 2-5 Keep Alive Power Source Selection



2•3•6 LXT970 Power Up HW Configuration

The LXT970 can be configure for power up by 9 pins 5 of them are connected to the LXT970 through DS1 (DS1 is a 16 pin contain 8 dip switches) they are the HW configuration pins. The pins MF0 - MF4 can configure the following options:
MF0 enables the autonegotiation, if DS1(1) is OFF it enable the autonegotiation
MF1 selects DTE or Repeater, if DS1(2) is ON it enable the DTE mode.
MF2 selects symbol (5B) or Nibble (4B) if DS1(3) is ON Nibble (4B) is selected.
MF3 enables scrambler operation, if DS1(4) is ON the scrambler operation is enabled.
MF4 select the output possibility options, twisted pair or the fiber optic.



DS1 Default Configuration.

2•4 INSTALLATION INSTRUCTIONS

The MPC860DB should be plugged into the MPC8XXFADS Mother Board. This should be done when the FADS is disconnected from any power supply. The 860DB should be placed over the mother board connectors in a way that the mother board connectors of the 860DB, PM1 - PM4 match the daughter connectors of the FADS and than pressed gently into position.

The connectors are arranged in a non symmetrical form, so miss-insertion is inhibited.

3 - OPERATING INSTRUCTIONS

3•1 INTRODUCTION

This chapter provides necessary information to use the MPC860DB

3•2 CONTROLS AND INDICATORS

The MPC860DB has in addition to the switches a few indicators - described below:.

3•2•1 GND Bridges

There are 4 GND bridges on the MPC860DB. They are meant to assist general measurements and logic-analyzer connection.

Warning

The GND bridges on board, physically resemble J4. Do not mistake J4 to be a GND jumper, otherwise, permanent damage might be inflicted to the MPC860DB and or to the MPC8XXFADS.

Warning

When connecting to a GND bridge, use only INSULATED GND clips. Failure in doing so, might result in permanent damage to the MPC860DB.

3•2•2 3.3V Indicator - LD1

The yellow 3.3V LED LD1 indicates that the 3.3V power bus is powered from the MPC8XXFADS.

3•2•3 Receive Led - LD2

When the yellow LED LD2 is ON, the fast ethernet receive is in process, for 10M or for 100M.

3•2•4 Transmit Led - LD3

When the yellow LED LD3 is ON, the fast ethernet transmit is in process, for 10M or for 100M.

3•2•5 Link Led - LD4

When the yellow LED LD4 is ON, during the 100Mbps operation, indicates scrambler lock and receipt of valid idle codes. During 10Mbps operation, indicates link valid status.

3•2•6 Collision Led - LD5

When the yellow LED LD5 is ON, in the default mode it indicates a collision. However this LED is a programmable led and it can indicate other definitions. For a programing options see configuration register, register 19 in the LXT970 user guide.

3•2•7 Speed Led- LD6

When the Speed LED LD6 is ON it indicates that the LXT970 operate in 100Mbps. When this LED is off it indicates that the ethernet speed is 10M. Note: the 10M ethernet means 10M operating through the MII bus.

3•2•8 Fast - Ethernet - On Indicator - LD7

When the yellow Fast - Ethernet-ON indicator LED LD7 is ON, it designates that the LXT970 transceiver is enabled for the Fast - Ethernet operation. When it is off, the LXT970 is tri-stated and the MII pins output from the LXT970 are in three-state. these pins with the input to the LXT970 pins may be used for any alternate function. See also TABLE 4-23. "BCSR4 Description" on page 57 of the MPC8XXFADS User's Manual.

3•3 MEMORY MAP

The memory map is identical to all daughter boards, therefore described in the MPC8XXFADS User's Manual - section 3•3 "MEMORY MAP" on page 16.

3•4 MPC Registers' Programming

See 3•4 "MPC Registers' Programming" on page 10 of the MPC8XXFADS User's Manual.

4 - Functional Description

In this chapter the various modules combining the MPC860DB are described in details.

4•1 Reset & Reset - Configuration

There are 3 reset sources for the MPC:

1) Power-On Reset[A]
2) Hard Reset
3) Soft Reset

4•1•1 Power-On Reset

The Power - On Reset on the MPC860DB is generated out of 2 alternative power buses:

1) The keep alive power bus
2) The MAIN power bus.

Selection between the 2 options is done by means of jumper.

When option (1) above is selected, the power-on reset is generated by a dedicated voltage detector made by Seiko the S-8051HN-CD-X with detection voltage range of 1.795 to 2.005V. During keep alive power-on or when there is a voltage drop of that input into the above range Power-On Reset is generated, i.e., PORESET* input of the MPC is asserted for a period of approximately 4 sec.

When option (2) above is selected, the power-on reset is generated by a dedicated voltage detector made by Seiko the S-8052ANY-NH-X with detection voltage range of 2.595V to 2.805V. During MAIN 3.3V bus power-on or when there is a voltage drop of that input into the above range Power-On Reset is generated, i.e., PORESET* input of the MPC is asserted for a period of approximately 4 sec. The MAIN power on reset also generates power-on reset to all logic located on the motherboard.

When PORESET* is asserted to the MPC, the Power-On reset configuration is made available to MPC. See 4•1•6•1 "Power - On Reset Configuration" on page 29 of MPC8XXFADS User's Manual.

4•1•2 Hard Reset

Hard Reset is generated to the MPC by the following sources:

1) The MAIN power-on reset
2) Manual Hard Reset generated on the mother board
3) The debug port Hard reset
4) and by MPC860's internal sources.

When the open-drain signal Hard Reset is asserted, Hard reset configuration is driven on the data bus by logic on the motherboard. See 4•1•6•2 "Hard Reset Configuration" on page 29 on MPC8XXFADS User's Manual.

4•1•3 Soft Reset

Soft Reset is generated to the MPC by the following sources:

1) The debug port controller located on the motherboard
2) Manual Soft Reset generated on the motherboard
3) and by MPC internal sources.

When Soft reset is generated to the MPC, Soft Reset configuration is made available to the MPC by logic residing

A. In fact generated on the daughter board.

over the motherboard. See 4•1•6•3 "Soft Reset Configuration" on page 29 on MPC8XXFADS User's Manual.

4•2 Interrupts

Two external interrupts are applied to the MPC via its interrupt controller the ABORT (NMI), which is generated by a push-button & logic residing over the motherboard, and the other is on the IRQ2 which is the interrupt of the LXT970 Fast Ethernet Tranceiver, if using a MPC860T device. If using a MPC860SAR and also using the MPC860SAR-PHY board the IRQ2~ signal is coming from this board. More details are in the MPC860SAR-PHY board user manual.

4•3 Clock Generator

Although most of clock generator logic is found on this board, it is documented within the motherboard User's Manual, since, it is common to all daughter boards. See 4•3 "Clock Generator" on page 30 of the MPC8XXFADS User's Manual.

4•4 Fast Ethernet Support
This section is relevant for 860T only.

The MPC860DB has on-board full support for 802.3 Media Independent Interface (MII), made by the Level One LXT970 device, the connection between the LXT970 and the line can be made by twisted pair RJ45 connector or by fiber optic connector which is optional.
The LXT970 used in the MPC860DB has the following features: it is a IEEE 802.3 Compatible which is a 10BASE-T and 100BASE-TX using a single RJ45 connector. It support an auto-negotiation via Fast Link Pulse (FLP) exchange and parallel detection for legacy 10BASE-T and 100BASE-TX systems. MII interface, 100BASE-FX fiber optic capable, configurable through the MII serial port, it can be DTE repeater or switch application.
The LXT970 has several control pins that can configure the mode of operation. These pins are separated to two pins groups, the WH control pins, and the SW control pins. The HW control pins are the MF(0:4) connected to the DS1, the SW control pins are the TRSTE, FDE and CFG(0:1) which are controlled via the BCSR4 register.
The following tables illustrate the LXT970 configuration options.

TABLE 4-1. MF0 - MF4 Function Description Pins

PIN NAME	*FUNCTION*	*DS1 ON CONDITION*	*DS1 OFF CONDITION*	*Default*
MF0	Auto-negotiation	Disable	Enable	Enable
MF1	Repiter/DTE mode	DTE	Repeater	DTE
MF2	Nibble 4B/Symbol 5B	Nibble 4B	Symbol 5B	Nibble 4B
MF3	Scrambler Operation	Enable	Disable	Enable
MF4	Select TX or FX	100TX	100FX	100TX

The following table describe the SW control pins controlled via the BCSR4 register which is on the mother board

TABLE 4-2. BCSR4 The control pins for the LXT970 relevant for MPC860T only

BIT	*MNEMONIC*	*FUNCTION*	*PON DEF*	*ATT.*
4	UUFEN~	When this signal is active (LOW) it enable the LXT970 device. This signal connected to the TRSTE signal of the LXT970. In DTE mode when this pin is high the LXT970 isolate itself from the MII data interface. In repeater mode when it is high the LXT970 tri state the MII output pins.	1	R,W
5	FETHCFG0	Fast Ethernet CFG0 signal When the LXT970 is in auto negotiation a low to high transition in this pin cause an auto negotiate to re-start. When the auto negotiation is disabled this input selects operating speed bit 0.13 When this pin is high the 100Mbps is selected 0.13 = 1. When this pin is low the 10Mbps is selected 0.13 = 0.	1	R,W
6	FETHFDE	Full Duplex Enable when auto negotiation is enable the FDE pin of the LXT970 determine full duplex advertisement capability in combination with MF4 and CFG1. See the LXT970 documentation. When auto negotiation is disable the FDE pin of the LXT970 effects full duplex and determines the value of bit 0.8 Duplex Mode. When this pin is high Full Duplex is Enable. 0.8 = 1. When this pin is low Full Duplex is Disable 0.8 = 0.	1	R,W
9	FETHCFG1	Fast Ethernet CFG1 signal When the LXT970 is in auto negotiation this pin determines operating speed advertisement capability in combination with MF4. see See the LXT970 documentation. When auto negotiation is disabled this input enables 10Mbps link test function and directly affects bit 19.8. When this pin is high, 10Mbps link test is disabled 19.8 = 1. When this pin is low, 10Mbps link test is enabled 19.8 = 0.	1	R,W
10	FETHRST~	Fast Ethernet Reset. When this pin active (LOW) signal is being asserted the Fast ethernet tranceiver is being reset.	1	R,W

The Fast Ethernet transceiver support two physical interfaces:

- RJ45 8pin connector for the twisted pair use. This connector is mounted on the board.
- Fiber Optic multi mode tranceiver not mounted on the board, it is an optional. The board is designed for the HP HFBR-5103 or HFBR-5105.

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4•5 Board Control & Status Register - BCSR

Most BCSR control signals and some of BCSR's status signals are available on the motherboard connectors and on the expansion connectors. The BCSR control most of the functions available on the MPC860DB and on the MPC8XXFADS.

See 4•11 "Board Control & Status Register - BCSR" on page 45 of MPC8XXFADS User's Manual.

5 - Support Information

In this chapter all information needed for support, maintenance and connectivity to the MPC860DB is provided.

5•1 Interconnect Signals

The MPC860DB interconnects with external devices via the following set of connectors:

1) P1, P2, P3, P4, P5, P6 and P8 - Logic Analyzer connectors
2) P9 RJ45 connector for the Fast Ethernet.
3) U3 Fiber Optic Tranceiver (Connector not mounted on the board).
4) PM1, PM2, PM3 and PM4 - Mother Board Connectors
5) PX1, PX2, PX3 & PX4 - Expansion Connectors
6) MPC8XXFADS's P8 - Serial Ports' Expansion Connector[A]

5•1•1 P1, P2, P3, P4, P5, P6 and P8 - Logic Analyzer Connectors

These connectors are 38 pin, receptacle MICTOR connectors made by AMP. Each connector connects to a dedicated adaptor for HP 16500 series of logic analyzer, which interconnects to two 16 bit pods. Since all the signals that appear on these connectors appear also on the mother-board connectors and on the expansion connectors, they are described there.

5•1•1•1 P1, P2, P3, P4, P5, P6 and P8 Signal Names

The Logic Analyzer connectors signal names table compose of the motherboard signal name and the MPC relevant special name if there is a special function to this pin the special name mentioned in the same MPC column in the table. For example for the MPC860SAR PB16 this pin name is also a PHREQ[0]. For MPC860T SPARE4 is now MIICOL. One column is for the Mother board signal name to make is easy to the user to follow the signals from the mother board to the daughter board.

A. This connector is located on the Mother Board. It is documented here since its contents depends on the Daughter Board.

TABLE 5-1 P1 Interconnect Signals

Pin#	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*MPC860Sar Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*	*Pin#*	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*MPC860Sar Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*
1	N.C.	N.C.	N.C.	N.C.	2	N.C.	N.C.	N.C.	N.C.
3	GND	GND	GND	GND	4	N.C.	N.C.	N.C.	N.C.
5	TS~	TS~	TS~	TS~	6	TA~	TA~	TA~	TA~
7	TS~	TS~	TS~	TS~	8	TA~	TA~	TA~	TA~
9	F_CS~	F_CS~	F_CS~	F_CS~	10	VFLS0	VFLS0	VFLS0	VFLS0
11	BCSRCS~	BCSRCS~	BCSRCS~	BCSRCS~	12	VFLS1	VFLS1	VFLS1	VFLS1
13	DRMCS1~	DRMCS1~	DRMCS1~	DRMCS1~	14	AT0	AT0	AT0	AT0
15	DRMCS2~	DRMCS2~	DRMCS2~	DRMCS2~	16	AT1	AT1	AT1	AT1
17	SDRMCS~	SDRMCS~	SDRMCS~	SDRMCS~	18	AT2	AT2	AT2	AT2
19	CS5~	CS5~	CS5~	CS5~	20	AT3	AT3	AT3	AT3
21	CS6~	CS6~	CS6~	CS6~	22	VF0	VF0	VF0	VF0
23	CS7~	CS7~	CS7~	CS7~	24	VF1	VF1	VF1	VF1
25	N.C.	N.C.	N.C.	N.C.	26	VF2	VF2	VF2	VF2
27	R_W~	R_W~	R_W~	R_W~	28	WAIT_B~	WAIT_B~	WAIT_B~	WAIT_B~
29	REG_A~	REG_A~	REG_A~	REG_A~	30	RESETA	RESETA	RESETA	RESETA
31	TSIZE1	TSIZE1	TSIZE1	TSIZE1	32	POE_A~	POE_A~	POE_A~	POE_A~
33	BURST~	BURST~	BURST~	BURST~	34	MODCK1	MODCK1	MODCK1	MODCK1
35	TEA~	TEA~	TEA~	TEA~	36	MODCK2	MODCK2	MODCK2	MODCK2
37	SPKROUT	SPKROUT (KR/ IRQ4~)	SPKROUT (KR/IRQ4~)	SPKROUT (KR/ IRQ4~)	38	EXTCLK	EXTCLK	EXTCLK	EXTCLK

TABLE 5-2. P2 - Interconnect Signals

Pin#	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*MPC860Sar Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*	*Pin#*	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*MPC860Sar Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*
1	N.C.	N.C.	N.C.	N.C.	2	N.C.	N.C.	N.C.	N.C.
3	GND	GND	GND	GND	4	N.C.	N.C.	N.C.	N.C.
5	NC	NC	NC	NC	6	BS0A~	BS0A~	BS0A~	BS0A~

TABLE 5-2. P2 - Interconnect Signals

Pin#	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*MPC860Sar Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*	*Pin#*	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*MPC860Sar Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*
7	ALE_A	ALE_A	ALE_A	ALE_A	8	BS0A~	BS0A~	BS0A~	BS0A~
9	CE1A~	CE1A~	CE1A~	CE1A~	10	BS1A~	BS1A~	BS1A~	BS1A~
11	CE2A~	CE2A~	CE2A~	CE2A~	12	BS2A~	BS2A~	BS2A~	BS2A~
13	BWAITA~	BWAITA~	BWAITA~	BWAITA~	14	BS3A~	BS3A~	BS3A~	BS3A~
15	BB~	BB~	BB~	BB~	16	WE0~	WE0~	WE0~	WE0~
17	BR~	BR~	BR~	BR~	18	WE1~	WE1~	WE1~	WE1~
19	BWP	BWP	BWP	BWP	20	WE2~	WE2~	WE2~	WE2~
21	BCD2~	BCD2~	BCD2~	BCD2~	22	WE3~	WE3~	WE3~	WE3~
23	BCD1~	BCD1~	BCD1~	BCD1~	24	DRM_W~	DRM_W~	DRM_W~	DRM_W~
25	BG~	BG~	BG~	BG~	26	EDOOE~	EDOOE~	EDOOE~	EDOOE~
27	BI~	BI~	BI~	BI~	28	GPL2~	GPL2~	GPL2~	GPL2~
29	BRDY	BRDY	BRDY	BRDY	30	GPL3~	GPL3~	GPL3~	GPL3~
31	BADDR28	BADDR28	BADDR28	BADDR28	32	GPL4A~	GPL4A~	GPL4A~	GPL4A~
33	BADDR29	BADDR29	BADDR29	BADDR29	34	GPL4B~	GPL4B~	GPL4B~	GPL4B~
35	BADDR30	BADDR30	BADDR30	BADDR30	36	GPL5A~	GPL5A~	GPL5A~	GPL5A~
37	AS~	AS~	AS~	AS~	38	GPL5B~	GPL5B~	GPL5B~	GPL5B~

TABLE 5-3. P3 - Interconnect Signals

Pin #	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*MPC860Sar Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*	*Pin #*	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*MPC860Sar Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*
1	N.C.	N.C.	N.C.	N.C.	2	N.C.	N.C.	N.C.	N.C.
3	GND	GND	GND	GND	4				
5	TEA~	TEA~	TEA~	TEA~	6				
7	A0	A0	A0	A0	8	A16	A16	A16	A16
9	A1	A1	A1	A1	10	A17	A17	A17	A17
11	A2	A2	A2	A2	12	A18	A18	A18	A18
13	A3	A3	A3	A3	14	A19	A19	A19	A19
15	A4	A4	A4	A4	16	A20	A20	A20	A20

Support Information

TABLE 5-3. P3 - Interconnect Signals

Pin #	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*MPC860Sar Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*	*Pin #*	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*MPC860Sar Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*
17	A5	A5	A5	A5	18	A21	A21	A21	A21
19	A6	A6	A6	A6	20	A22	A22	A22	A22
21	A7	A7	A7	A7	22	A23	A23	A23	A23
23	A8	A8	A8	A8	24	A24	A24	A24	A24
25	A9	A9	A9	A9	26	A25	A25	A25	A25
27	A10	A10	A10	A10	28	A26	A26	A26	A26
29	A11	A11	A11	A11	30	A27	A27	A27	A27
31	A12	A12	A12	A12	32	A28	A28	A28	A28
33	A13	A13	A13	A13	34	A29	A29	A29	A29
35	A14	A14	A14	A14	36	A30	A30	A30	A30
37	A15	A15	A15	A15	38	A31	A31	A31	A31

TABLE 5-4. P4 - Interconnect Signals

Pin #	*Mother Board Signal Name*	*Daughter Board Signal Name*	*Daughter Board Signal Name*	*Daughter Board Signal Name*	*Pin #*	*Mother Board Signal Name*	*MPC860TDaughtr Board Signal Name*	*860SAR Daughter Signal Name*	*MPC860 Daughter Board Signal Name*
1	N.C.	N.C.	N.C.	N.C.	2	N.C.	N.C.		
3	GND	GND	GND	GND	4				
5	N.C.	N.C.	N.C.	N.C.	6	LD1	MIIRXCLK		PD8
7	PA0	PA0	PA0	PA0	8	LD8	MIIRXD3	UTPB0	PD15
9	PA1	PA1	PA1	PA1	10	LD7	MIIRXD2	UTPB1	PD14
11	PA2	PA2	PA2	PA2	12	LD6	MIIRXD1	UTPB2	PD13
13	PA3	PA3	PA3	PA3	14	LD5	MIIMDC	UTPB3	PD12
15	PA4	PA4	PA4	PA4	16	LD4	MIITXER	RxEnb~	PD11
17	PA5	PA5	PA5	PA5	18	LD3	MIIRXD0	TxEnb~	PD10
19	PA6	PA6	PA6	PA6	20	LD2	MIITXD0	UTPclk	PD9
21	PA7	PA7	PA7	PA7	22	LD1	MIIRXCLK	PD8	PD8
23	PA8	PA8	PA8	PA8	24	LD0	MIIRXER	UTPB4	PD7
25	PA9	PA9	PA9	PA9	26	LOE	MIIRXDV	UTPB5	PD6
27	PA10	PA10	PA10	PA10	28	VSYNC	MIITXD3	UTPB6	PD5
29	PA11	PA11	PA11	PA11	30	HSYNC	MIITXD2	UTPB7	PD4
31	IRDTXD	IRDTXD	IRDTXD	IRDTXD	32	SHIFT_C	MIITXD1	SOC	PD3
33	IRDRXD	IRDRXD	IRDRXD	IRDRXD	34	SPARE1	MIICRS	SPARE1	SPARE1
35	ETHTX	ETHTX	ETHTX	ETHTX	36	SPARE2	MIIMDIO	SPARE2	SPARE2
37	ETHRXS	ETHRXS	ETHRXS	ETHRXS	38	SPARE3	MIITXEN	SPARE3	SPARE3

TABLE 5-5. P5 - Interconnect Signals

Pin #	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*860SAR Daughter Signal Name*	*860 Daughter Board Signal Name*	*Pin #*	*Mother Board Signal Name*	*860T Daughter & Board Signal Name*	*860SAR Signal Name*	*860 Daughter Board Signal Name*
1	N.C.	N.C.	N.C.	N.C.	2	N.C.	N.C.	N.C.	N.C.
3	GND	GND	GND	GND	4				
5	IRQ7~	MIITCLK	IRQ7~	IRQ7~	6				
7	UUFEN~	UUFEN~ (DB ONLY)			8	DSDI	DSDI	DSDI	DSDI

TABLE 5-5. P5 - Interconnect Signals

Pin #	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*860SAR Daughter Signal Name*	*860 Daughter Board Signal Name*	*Pin #*	*Mother Board Signal Name*	*860T Daughter & Board Signal Name*	*860SAR Signal Name*	*860 Daughter Board Signal Name*
9	FETHFDE	FETHFDE(DB ONLY)			10	DSCK	DSCK	DSCK	DSCK
11	FETHCFG1	FETHCFG1 (DB ONLY)			12	DSDO	DSDO	DSDO	DSDO
13	FETHCFG0	FETHCFG0 (DB ONLY)			14	TMS	TMS	TMS	TMS
15	FETHRST~	FETHRST~ (DB ONLY)			16	TRST~	TRST~	TRST~	TRST~
17	BVS1	BVS1	BVS1	BVS1	18	NMI~	NMI~	NMI~	NMI~
19	BVS2	BVS2	BVS2	BVS2	20	IRQ1~	IRQ1~	IRQ1~	IRQ1~
21	BBVD1	BBVD1	BBVD1	BBVD1	22	IRQ2~	IRQ2~	IRQ2~	IRQ2~
23	BBVD2	BBVD2	BBVD2	BBVD2	24	IRQ3~	IRQ3~	IRQ3~	IRQ3~
25	RSTCNF~	RSTCNF~	RSTCNF~	RSTCNF~	26	FRZ	FRZ	FRZ	FRZ
27	TEXP	TEXP	TEXP	TEXP	28	BINPAK~	BINPAK~	RxCav	BINPAK~
29	HRESET~	HRESET~	HRESET~	HRESET~	30	DP0	DP0	DP0	DP0
31	SRESET~	SRESET~	SRESET~	SRESET~	32	DP1	DP1	DP1	DP1
33	PORST~	PORST~	PORST~	PORST~	34	DP2	DP2	DP2	DP2
35	R_PORI~	R_PORI~	R_PORI~	R_PORI~	36	DP3	DP3	DP3	DP3
37	IRQ7~	MIITCLK	IRQ7~	IRQ7~	38		V3.3	V3.3	V3.3

TABLE 5-6. P6 - Interconnect Signals

Pin #	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*860SAR Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*	*Pin #*	*Mother Board Signal Name*	*860T Daughter Board Signal Name*	*860SAR Daughter Board Signal Name*	*860 Daughter Board Signal Name*
1	N.C.	N.C.	N.C.	N.C.	2	N.C.	N.C.	N.C.	N.C.
3	GND	GND	GND	GND	4	N.C.	N.C.	N.C.	N.C.
5	N.C.	N.C.	N.C.	N.C.	6	SYSCLK	SYSCLK	SYSCLK	SYSCLK
7	PB14	PB14	PB14	PB14	8	SYSCLK	SYSCLK	SYSCLK	SYSCLK
9	PB15	PB15	TxCav	PB15	10	PB30	PB30	PB30	PB30
11	PB16	PB16	PHREQ[0]	PB16	12	PB31	PB31	PB31	PB31
13	PB17	PB17	PHREQ[1]	PB17	14	PC4	PC4	PC4	PC4
15	PB18	PB18	PB18	PB18	16	PC5	PC5	PC5	PC5

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TABLE 5-6. P6 - Interconnect Signals

Pin #	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*860SAR Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*	*Pin #*	*Mother Board Signal Name*	*860T Daughter Board Signal Name*	*860SAR Daughter Board Signal Name*	*860 Daughter Board Signal Name*
17	E_TENA	E_TENA	E_TENA	E_TENA	18	PC6	PC6	PC6	PC6
19	RSRXD2	RSRXD2	RSRXD2/ PHSEL[0]	RSRXD2	20	PC7	PC7	PC7	PC7
21	RSTXD2	RSTXD2	RSTXD2/ PHSEL[1]	RSTXD2	22	PC8	PC8	PC8	PC8
23	RSDTR2~	RSDTR2~	RSDTR2~	RSDTR2~	24	PC9	PC9	PC9	PC9
25	RSDTR1~	RSDTR1~	RSDTR1~	RSDTR1~	26	E_RENA	E_RENA	E_RENA	E_RENA
27	RSRXD1	RSRXD1	RSRXD1	RSRXD1	28	E_CLSN	E_CLSN	E_CLSN	E_CLSN
29	RSTXD1	RSTXD1	RSTXD1	RSTXD1	30	PC12	PC12	PC12	PC12
31	PB26	PB26	PB26	PB26	32	PC13.	PC13.	PC13.	PC13.
33	PB27	PB27	PB27	PB27	34	PC14	PC14	PC14	PC14
35	PB28	PB28	PB28	PB28	36	SPARE4	MIICOL	SPARE4	SPARE4
37	PB29	PB29	PB29	PB29	38	N.C.	N.C.	N.C.	N.C.

TABLE 5-7. P8 - Interconnect Signals

Pin #	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*680SAR Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*	*Pin #*	*Mother Board Signal Name*	*MPC860TD aughter Board Signal Name*	*860SAR Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*
1	N.C.	N.C.	N.C.	N.C.	2	N.C.	N.C.	N.C.	N.C.
3	GND	GND	GND	GND	4	N.C.	N.C.	N.C.	N.C.
5	N.C.	N.C.	N.C.	N.C.	6	N.C.	N.C.	N.C.	N.C.
7	D0	D0	D0	D0	8	D16	D16	D16	D16
9	D1	D1	D1	D1	10	D17	D17	D17	D17
11	D2	D2	D2	D2	12	D18	D18	D18	D18
13	D3	D3	D3	D3	14	D19	D19	D19	D19
15	D4	D4	D4	D4	16	D20	D20	D20	D20
17	D5	D5	D5	D5	18	D21	D21	D21	D21
19	D6	D6	D6	D6	20	D22	D22	D22	D22
21	D7	D7	D7	D7	22	D23	D23	D23	D23
23	D8	D8	D8	D8	24	D24	D24	D24	D24

TABLE 5-7. P8 - Interconnect Signals

Pin #	*Mother Board Signal Name*	*MPC860T Daughter Board Signal Name*	*680SAR Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*	*Pin #*	*Mother Board Signal Name*	*MPC860TDaughter Board Signal Name*	*860SAR Daughter Board Signal Name*	*MPC860 Daughter Board Signal Name*
25	D9	D9	D9	D9	26	D25	D25	D25	D25
27	D10	D10	D10	D10	28	D26	D26	D26	D26
29	D11	D11	D11	D11	30	D27	D27	D27	D27
31	D12	D12	D12	D12	32	D28	D28	D28	D28
33	D13	D13	D13	D13	34	D29	D29	D29	D29
35	D14	D14	D14	D14	36	D30	D30	D30	D30
37	D15	D15	D15	D15	38	D31	D31	D31	D31

5•1•2 P9 & U3 - Fast Ethernet Connectors Relevant only for MPC860T

The 860DB supports both types of connectors for fast ethernet RJ45 (P9) and fiber optic tranceiver (it is not mounted on the board) U3. The signals of P9 are described in TABLE 5-8. "P9 Interconnect Signal" below:

TABLE 5-8. P9 Interconnect Signal

Pin No.	*Signal Name*
1	TPO-
2	TPO+
3	TPI+
4	COMMON_O
5	COMMON_O
6	TPI-
7	COMMON_I
8	COMMON_I

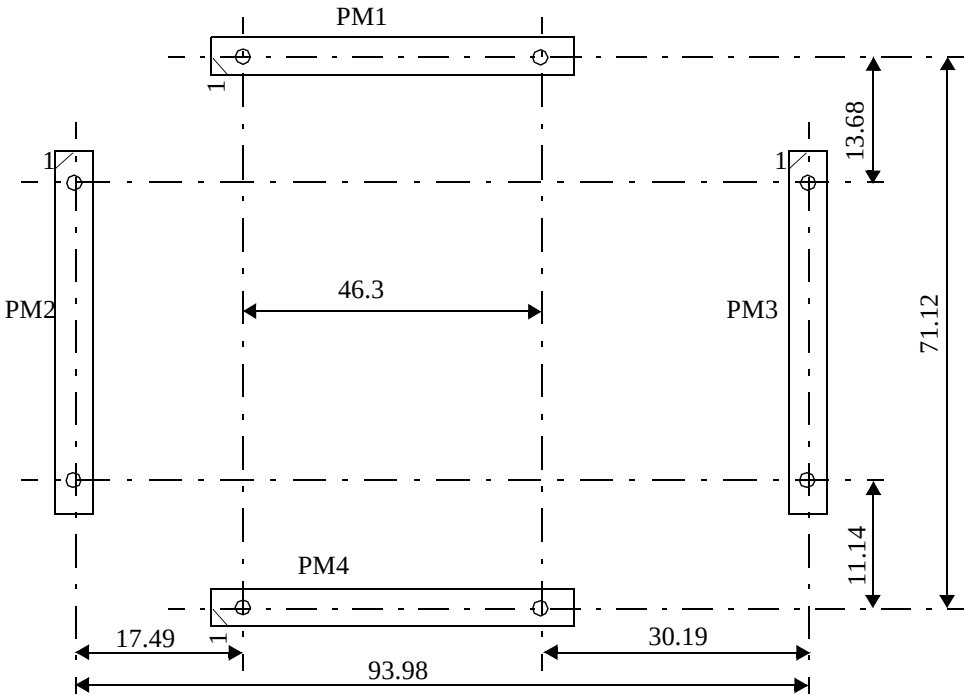
5•1•3 PM1 - PM4, Mother Board Connectors

These connectors which connect to their mates on the motherboard (hence their name) are 140 pin inter-board, mail connectors made by Molex. These connectors are arranged in a quadratic shape, this to provide the shortest PCB routes as possible. As can be seen from their mechanical assembly shown in FIGURE 5-1 "Motherboard Connectors Mechanical Assembly" below - the connectors are not set in a perfect symmetric shape, this, to prevent the possibility of daughter-board's miss-insertion.

5•1•3•1 PM1 - PM4 Signal Names

The Mother Board connectors signal names table compose of the motherboard signal name and the MPC relevant special name if there is a special function to this pin. The special name mentioned in the same MPC column in the table. For example for the MPC860SAR PB16 this pin name is also a PHREQ[0]. For MPC860T SPARE4 is now MIICOL. One column is for the Mother board signal name to make is easy to the user to follow the signals from the mother board to the daughter board.

FIGURE 5-1 Motherboard Connectors Mechanical Assembly[A B]



The motherboard connectors's signals are described in TABLE 5-9. "PM1 Interconnect Signals" on page 29., TABLE 5-10. "PM2 Interconnect Signals" on page 28. TABLE 5-11. "PM3 Interconnect Signals" on page 45 and TABLE 5-

A. Top View (from Component side)
B. All measures are in mm.

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12. "PM4 Interconnect Signals" on page 54.TABLE 5-13. "PX1 - PM1 Interconnect Signals' Differences" on page 61

TABLE 5-9. PM1 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
1	BB~	BB~	BB~	BB~	I/O, L	MPC's Bus Busy signal. Pulled - up on the FADS.
2	VCC	VCC	VCC	VCC	-	
3	DRM_W~	DRM_W~	DRM_W~	DRM_W~	I,L	MPC's GPL0~ lines used as R/W~ signal for the DRAM simm or as A10 line for the SDRAM.
4	VCC	VCC	VCC	VCC	-	5V Bus.
5	TEA~	TEA~	TEA~	TEA~	I/O, L, O.D.	Transfer Error Acknowledge. Pulled-up, not driven on board.
6	VCC	VCC	VCC	VCC		
7	BR~	BR~	BR~	BR~	I/ O,L	MPC's Bus Request signal. Pulled - up on the FADS, but otherwise unused.
8	VCC	VCC	VCC	VCC		
9	BURST~	BURST~	BURST~	BURST~	I/O, L	MPC's Burst indication. Pulled - up on the FADS, but otherwise unused.
10	VCC	VCC	VCC	VCC		
11	GPL4A~	GPL4A~	GPL4A~	GPL4A~	X,L	UPMA general purpose line 4. Not used on the FADS.
12	VCC	VCC	VCC	VCC		
13	TA~	TA~	TA~	TA~	I/O, L	MPC's transfer Acknowledge signal. Indicates end of bus cycle, used with FADS logic.
14	VCC	VCC	VCC	VCC		
15	TS~	TS~	TS~	TS~	I/O, L	MPC's Transfer Start indication. Pulled - up, but otherwise unused on the FADS.
16	VCC	VCC	VCC	VCC		
17	GPL5B~	GPL5B~	GPL5B~	GPL5B~	O, L	General Purpose Line 5 of UPMB. Not used on the FADS.
18	VCC	VCC	VCC	VCC		
19	BG~	BG~	BG~	BG~	I/O, L	MPC's Bus grant signal. Pulled - up on the FADS, but otherwise unused.
20	VCC	VCC	VCC	VCC		
21	GPL4B~	GPL4B~	GPL4B~	GPL4B~	O, L	General Purpose Line 4 of UPMB. Not used on the FADS.
22	VCC	VCC	VCC	VCC		

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TABLE 5-9. PM1 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
23	R_W~	R_W~	R_W~	R_W~	I/O, L	MPC's Read/Write~ indication. Pulled - up on the FADS and used by FADS logic.
24	VCC	VCC	VCC	VCC		
25	BCSRCS~	BCSRCS~	BCSRCS~	BCSRCS~	I/O, L	In fact CS1~ of the MPC. Used as chip-select for the BCSRs. Pulled - up. When BCSR is removed from the local map, may be used off-board via the daughter-board's expansion connectors.
26	VCC	VCC	VCC	VCC	O	5V Bus.
27	GPL5A~	GPL5A~	GPL5A~	GPL5A~	X,L	UPMA general purpose line 5. Not used on the FADS.
28	VCC	VCC	VCC	VCC	O	5V Bus.
29	BI~	BI~	BI~	BI~	I/ O,L	MPC's Burst Inhibit input. Pulled - up, but otherwise unused on the FADS.
30	N.C.	N.C.	N.C.	N.C.	-	Not Connected. Reserved.
31	CS7~	CS7~	CS7~	CS7~		
32	GND	GND	GND	GND	-	FADS Ground plane.
33	CS5~	CS5~	CS5~	CS5~	-	MPC's Chip Select line 5. Unused on the FADS.
34	GND	GND	GND	GND		
35	CE1A~	CE1A~	CE1A~	CE1A~	I, L	PC-Card Enable 1 for PCMCIA slot A. Enables the EVEN address bytes. Used by on-board PCMCIA port.
36	GND	GND	GND	GND		
37	F_CS~	F_CS~	F_CS~	F_CS~	I/O, L	In fact MPC's chip-select line 0. Used as chip-select for the Flash Simm. Pulled - up. When the Flash is disabled via BCSR, may be used off-board via the daughter-board's expansion connectors.
38	GND	GND	GND	GND		
39	CS6~	CS6~	CS6~	CS6~	-	MPC's Chip Select line 6. Unused on the FADS.
40	GND	GND	GND	GND		
41	CE2A~	CE2A~	CE2A~	CE2A~	I, L	PC-Card Enable 2 for PCMCIA slot A. Enables the ODD address bytes. Used by on-board PCMCIA port.
42	GND	GND	GND	GND		
43	DRMCS2~	DRMCS2~	DRMCS2~	DRMCS2~	I/O, L	In fact MPC's chip-select line 3. Used as chip-select line for the 2'nd bank of the Dram Simm. Pulled - up. When the Dram is disabled via BCSR or when a single-bank Dram Simm is being used - may be used off-board via the daughter board's expansion connectors.
44	GND	GND	GND	GND		

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TABLE 5-9. PM1 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
45	DRMCS1~	DRMCS1~	DRMCS1~	DRMCS1~	I/O, L	In fact MPC's chip-select line 2. Used as chip-select line for the 1'st bank of the Dram Simm. Pulled - up. When the Dram is disabled via BCSR - may be used off-board via the daughter board's expansion connectors.
46	GND	GND	GND	GND		
47	SDRMCS~	SDRMCS~	SDRMCS~	SDRMCS~	I/O, L	In fact MPC's chip-select line 4. Used as chip-select for the Synchronous Dram. Pulled - up. When the SDRAM is disabled via BCSR, may be used off-board via the daughter board
48	GND	GND	GND	GND		
49	GPL3~	GPL3~	GPL3~	GPL3~	I/O, L	UPMA or UPMB general purpose line 3. Used as WR~ signal for the SDRAM.
50	GND	GND	GND	GND		
51	GPL2~	GPL2~	GPL2~	GPL2~	I, L	General Purpose Line 2 for UPMA or UPMB. Used with the SDRAM, as a CAS~ signal.
52	GND	GND	GND	GND		
53	WE3~	WE3~	WE3~	WE3~	I, L	GPCM Write Enable 3 or PCMCIA WE~. Selects the LSB within a word for the Flash Simm or qualifies Writes for the PC-Card.
54	GND	GND	GND	GND		
55	WE2~	WE2~	WE2~	WE2~	I, L	GPCM Write Enable 2 or PCMCIA OE~. Selects the offset 2 Byte within a word for the Flash Simm or open data buffers for read from PC-Card.
56	GND	GND	GND	GND		
57	WE1~	WE1~	WE1~	WE1~	I, L	GPCM Write Enable1 or PCMCIA I/O Write. Used to qualify write cycles to the Flash memory and as I/O Write for the PCMCIA channel.
58	GND	GND	GND	GND		
59	BS2A~	BS2A~	BS2A~	BS2A~	I, L	Byte Select 2 for UPMA. Selects offset 2 bytes within Word. Used for Dram access.
60	GND	GND	GND	GND		
61	WE0~	WE0~	WE0~	WE0~	I, L	GPCM Write Enable 0 or PCMCIA I/O Read. Used to qualify write cycles to the Flash memory and as I/O Reads from PC-Card.
62	GND	GND	GND	GND		

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TABLE 5-9. PM1 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
63	SPARE1	SPARE1	MIICRS	SPARE1	I,O, L	MPC spare line 1. Pulled - up but otherwise unused on the FADS. This signal is used only in MPC860T as a MIICRS signal
64	GND	GND	GND	GND		
65	EDOOE~	EDOOE~	EDOOE~	EDOOE~	I,L	In fact UPMA or UPMB General Purpose Line 1. Used for Output Enable with EDO Dram simms, which have this input (most of them don't). Used also as RAS signal for the SDRAM.
66	GND	GND	GND	GND		
67	BS0A~	BS0A~	BS0A~	BS0A~	I, L	Byte Select 0 from UPMA. Selects offset 0 Bytes within a word. Used as one of the CAS~ lines for Dram access.
68	GND	GND	GND	GND		
69	BS3A~	BS3A~	BS3A~	BS3A~	I, L	Byte Select 3 from UPMA. Selects offset 3 Bytes within a word. Used as one of the CAS~ lines for Dram access.
70	GND	GND	GND	GND		
71	A31	A31	A31	A31	I, T.S.	MPC's Address line 31.
72	GND	GND	GND	GND		
73	BS1A~	BS1A~	BS1A~	BS1A~	I, L	Byte Select 1 from UPMA. Selects offset 1 Bytes within a word. Used as one of the CAS~ lines for Dram access.
74	GND	GND	GND	GND		
75	TSIZ1	TSIZ1	TSIZ1	TSIZ1	x, T.S.	Transfer Size 1. Used in conjunction with TSIZ0 to indicate the number of bytes remaining in an operand transfer. Not used on the FADS.
76	GND	GND	GND	GND		
77	REG_A~	REG_A~	REG_A~	REG_A~	I, T.S., L	In fact TSIZ0/REG~. Transfer Size 0 or PCMCIA slot A REG~. Used with the PCMCIA port as Attribute memory select or I/O space select.
78	GND	GND	GND	GND		
79	A30	A30	A30	A30	I, T.S.	MPC's Address line 30.
80	GND	GND	GND	GND		
81	A21	A21	A21	A21	I, T.S.	MPC's Address line 21.
82	GND	GND	GND	GND		

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TABLE 5-9. PM1 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
83	A20	A20	A20	A20	I, T.S.	MPC's Address line 20.
84	GND	GND	GND	GND		
85	A7	A7	A7	A7	I, T.S.	MPC's Address line 7.
86	GND	GND	GND	GND		
87	A15	A15	A15	A15	I, T.S.	MPC's Address line 15.
88	GND	GND	GND	GND		
89	A14	A14	A14	A14	I, T.S.	MPC's Address line 14.
90	GND	GND	GND	GND		
91	A13	A13	A13	A13	I, T.S.	MPC's Address line 13.
92	GND	GND	GND	GND		
93	A6	A6	A6	A6	I, T.S.	MPC's Address line 6.
94	GND	GND	GND	GND		
95	A12	A12	A12	A12	I, T.S.	MPC's Address line 12.
96	GND	GND	GND	GND		
97	A11	A11	A11	A11	I, T.S.	MPC's Address line 11.
98	GND	GND	GND	GND		
99	A19	A19	A19	A19	I, T.S.	MPC's Address line 19.
100	GND	GND	GND	GND		
101	A9	A9	A9	A9	I, T.S.	MPC's Address line 9.
102	GND	GND	GND	GND		
103	A18	A18	A18	A18	I, T.S.	MPC's Address line 18.
104	GND	GND	GND	GND		
105	A10	A10	A10	A10	I, T.S.	MPC's Address line 10.

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TABLE 5-9. PM1 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
106	GND	GND	GND	GND		
107	A17	A17	A17	A17	I, T.S.	MPC's Address line 17.
108	GND	GND	GND	GND		
109	A16	A16	A16	A16	I, T.S.	MPC's Address line 16.
110	GND	GND	GND	GND		
111	A8	A8	A8	A8	I, T.S.	MPC's Address line 8.
112	GND	GND	GND	GND		
113	A29	A29	A29	A29	I, T.S.	MPC's Address line 29.
114	GND	GND	GND	GND		
115	A27	A27	A27	A27	I, T.S.	MPC's Address line 27.
116	GND	GND	GND	GND		
117	A28	A28	A28	A28	I, T.S.	MPC's Address line 28.
118	GND	GND	GND	GND		
119	A26	A26	A26	A26	I, T.S.	MPC's Address line 26.
120	GND	GND	GND	GND		
121	A25	A25	A25	A25	I, T.S.	MPC's Address line 25.
122	GND	GND	GND	GND		
123	A24	A24	A24	A24	I, T.S.	MPC's Address line 24.
124	GND	GND	GND	GND		
125	A22	A22	A22	A22	I, T.S.	MPC's Address line 22.
126	GND	GND	GND	GND		
127	A3	A3	A3	A3	I, T.S.	MPC's Address line 3. Not used on the FADS.
128	GND	GND	GND	GND		

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TABLE 5-9. PM1 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
129	A23	A23	A23	A23	I, T.S.	MPC's Address line 23.
130	GND	GND	GND	GND		
131	A4	A4	A4	A4	I, T.S.	MPC's Address line 4. Not used on the FADS.
132	GND	GND	GND	GND		
133	A2	A2	A2	A2	I, T.S.	MPC's Address line 2. Not used on the FADS.
134	GND	GND	GND	GND		
135	A5	A5	A5	A5	I, T.S.	MPC's Address line 5. Not used on the FADS.
136	GND	GND	GND	GND		
137	A1	A1	A1	A1	I, T.S.	MPC's Address line 1. Not used on the FADS.
138	GND	GND	GND	GND		
139	A0	A0	A0	A0	I, T.S.	MPC's Address line 0. Not used on the FADS.
140	GND	GND	GND	GND		

TABLE 5-10. PM2 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
1	V12	V12	V12	V12	O	10V output from voltage doubler. Used to switch TMOS gates on both mother and daughter boards. Should not be used for any other purpose.
2						
3						
4						
5	N.C.	N.C.	N.C.	N.C.		
6						

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TABLE 5-10. PM2 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
7	DSDI	DSDI	DSDI	DSDI	I/O	DSDI/TDI. Debug Port Serial Data Input or JTAG port serial Data Input. Used on the FADS as debug port serial data, driven by the debug-port controller. If the ADI bundle is not connected to the FADS, may be driven by external debug / JTAG[a] port controller.
8	GND	GND	GND	GND		
9						
10	DSCK	DSCK	DSCK	DSCK	I/O	DSCK/TCK. Debug Port Serial Clock input or JTAG port serial clock input. Used on the FADS as debug port serial clock, driven by the debug-port controller. If the ADI bundle is not connected to the FADS, may be driven by an external debug / JTAG[a] port controller.
11	DSDO	DSDO	DSDO	DSDO	I	DSDO/TDO. Debug Port Serial Data Output or JTAG port Data Output. Used on the FADS as debug port serial data. If the ADI bundle is not connected to the FADS, may be used by an external debug / JTAG[a] port controllers.
12	GND	GND	GND	GND		
13						
14	AT2	AT2	AT2	AT2	I/O	IP_B2/IOIS16~/AT2. PCMCIA slot B Input Port 2 or PCMCIA 16 bit I/O capability indication or Address Type 2.
15	GND	GND	GND	GND		
16	VF2	VF2	VF2	VF2	I/O	IP_B3/IWP2/VF2. PCMCIA slot B Input Port 3 or Instruction Watch-Point 2 or Visible Instruction Queue Flushes Status 2.
17	GND	GND	GND	GND		
18	VF0	VF0	VF0	VF0	I/O	IP_B4/LWP0/VF0. PCMCIA slot B Input Port 4 or Data Watch-Point 0 or Visible Instruction Queue Flushes Status 0.
19	GND	GND	GND	GND		
20						
21						
22	IRQ3~	IRQ3~	IRQ3~	IRQ3~	I/O, L	IRQ3~/CR~. MPC's interrupt request 3 or Cancel Reservation. Pulled - up but otherwise not used on the FADS.
23	GND	GND	GND	GND		

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TABLE 5-10. PM2 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
24	FRZ	FRZ	FRZ	FRZ	I, X	Freeze / IRQ6~. MPC debug state indication or Interrupt request line 6. Used by the debug port controller as debug state indication. May be configured to alternate function provided that VFLS(0:1) function as VFLS and J1 is moved to position 1-2.
25	GND	GND	GND	GND		
26	IRQ2~	IRQ2~	IRQ2~	IRQ2~	I/O, L	RSV~/IRQ2~. Reservation or Interrupt Request 2. Pulled - up but otherwise unused on the FADS. This signal used as an input pin for getting the interrupt from the PHY board when using 860SAR device and connecting the mother board to 860SAR-PHY board.
27	GND	GND	GND	GND		
28						
29						
30	AT3	AT3	AT3	AT3	I/O	IP_B7/PTR/AT3. PCMCIA slot B Input Port 7 or Program Trace (instruction fetch indication or Address Type 3.
31	GND	GND	GND	GND		
32	SPARE4	SPARE4	MIICALL	SPARE4	I/O	MPC's spare line 4. Pulled - up but otherwise unused on the FADS. This Signal is used in 860T only as a MIICALL signal for the Fast Ethernet
33	GND	GND	GND	GND		
34	VFLS0	VFLS0	VFLS0	VFLS0	I/O	IP_B0/IWP0/VFLS0. PCMCIA slot B Input Port 0 or Instruction Watchpoint 0 or Visible history Flushes Status 0. Configured as VFLS0. May be configured to any alternate function. Indicates in conjunction with VFLS1, the number of instructions flushed from the core's history buffer. Indicates also whether the MPC is in debug mode. If not using the debug port, may be configured for alternate function.
35	GND	GND	GND	GND		
36	SPKROUT	SPKROUT	SPKROUT	SPKROUT	I, X	KR~/IRQ4~/SPKROUT. Kill Reservation input or Interrupt Request 4 input or PCMCIA Speaker Output. Configured on the FADS as SPKROUT. May be configured to alternate function.
37	GND	GND	GND	GND		

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TABLE 5-10. PM2 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
38	VFLS1	VFLS1	VFLS1	VFLS1	I/O	IP_B1/IWP1/VFLS1. PCMCIA slot B Input Port 1 or Instruction Watchpoint 1 or Visible history Flushes Status 1. Configured as VFLS0. May be configured. Indicates in conjunction with VFLS1, the number of instructions flushed from the core's history buffer. Indicates also whether the MPC is in debug mode. If not using the debug port, may be configured for alternate function.
39	GND	GND	GND	GND		
40						
41						
42	VF1	VF1	VF1	VF1	-	IP_B5/LWP1/VF1. PCMCIA slot B Input Port 5 or Load/Store Watch-Point 1 or Visible Instruction Queue Flushes Status 1. Configured as VF1. May be configured to any alternate function as no use is done with it on the FADS.
43	GND	GND	GND	GND		
44	AT1	AT1	AT1	AT1	-	ALE_B/DSCK/AT1. Address Latch Enable for PCMCIA slot B or Debug Serial Clock or Address Type 1. Configured as ALE_B for all other daughter boards configured as AT1. Not used on the FADS. May be configured to any alternate function.
45	GND	GND	GND	GND		
46	AT0	AT0	AT0	AT0	I	IP_B6/DSDI/AT0. Input Port B 6 or Debug Serial Data Input or Address Type 0. Configured as a AT0. May be used for alternate function.
47	GND	GND	GND	GND		
48	POE_A~	POE_A~	POE_A~	POE_A~	I, L	In fact OP1 of the PCMCIA I/F. Enables address buffers towards the PC-Card.
49	GND	GND	GND	GND		
50						
51						
52	BADDR30	BADDR30	BADDR30	BADDR30	I/O,X	Burst Address Line 30. Dedicated for external master support. Used to generate Burst address during external master burst cycles. Pulled - up but otherwise unused on the FADS.
53	GND	GND	GND	GND		

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TABLE 5-10. PM2 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
54	ALE_A	ALE_A	ALE_A	ALE_A	I, H	Address Latch Enable for PCMCIA slot A. Latches address in external latches at the beginning of access to a PC-Card.
55	GND	GND	GND	GND		
56	BADDR29	BADDR29	BADDR29	BADDR29	I/O,X	Burst Address Line 29. Dedicated for external master support. Used to generate Burst address during external master burst cycles. Pulled - up but otherwise unused on the FADS.
57	GND	GND	GND	GND		
58	AS~	AS~	AS~	AS~	I/O, L	Asynchronous external master Address Strobe signal. When asserted (L) by the external master, the MPC recognizes an asynchronous cycle in progress. Pulled - up but otherwise unused on the FADS.
59	GND	GND	GND	GND		
60	MODCK1	MODCK1	MODCK1	MODCK1	I/O	OP2/MODCK1/STS~. PCMCIA Output Port 2 or Mode Clock 1 input or Special Transfer Start output. Used at Power-On reset as MODCK1. Configured afterwards as STS~.
61	GND	GND	GND	GND		
62	RESETA	RESETA	RESETA	RESETA	I,H	PC-Card reset signal.
63	GND	GND	GND	GND		
64						
65						
66	BADDR28	BADDR28	BADDR28	BADDR28	I/O,X	Burst Address Line 28. Dedicated for external master support. Used to generate Burst address during external master burst cycles. Pulled - up but otherwise unused on the FADS.
67	GND	GND	GND	GND		
68	TEXP	TEXP	TEXP	TEXP	X,X	MPC Timer Expired. Not used on the FADS.
69	GND	GND	GND	GND		
70	WAIT_B~	WAIT_B~	WAIT_B~	WAIT_B~	I/O, L	This signal is PCMCIA slot B wait signal. Pulled-up but otherwise not used on the FADS.
71	GND	GND	GND	GND		

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TABLE 5-10. PM2 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
72	MODCK2	MODCK2	MODCK2	MODCK2	I/O	OP3/MODCK2/DSDO. PCMCIA Output Port 3 or Mode Clock 2 input or Special Transfer Start output. Used at Power-On reset as MODCK2 and configured afterwards as a OP3. May be used with alternate function.
73	GND	GND	GND	GND		
74						
75						
76	N.C.	N.C.	N.C.	N.C.		
77	GND	GND	GND	GND		
78						
79						
80	SRESET~	SRESET~	SRESET~	SRESET~	I/O, L, O.D.	MPC Soft Reset. Driven by on-board logic and may be driven by off-board logic with Open-Drain gate only.
81	GND	GND	GND	GND		
82	PORST~	PORST~	PORST~	PORST~	X, L	Power On reset for the MPC. Not used on the FADS, generated on the daughter boards
83	GND	GND	GND	GND		
84	HRESET~	HRESET~	HRESET~	HRESET~	I/O, L, O.D.	MPC Hard Reset. Driven by on-board logic and may be driven by off-board logic with Open-Drain gate only.
85	GND	GND	GND	GND		
86	RSTCNF~	RSTCNF~	RSTCNF~	RSTCNF~	O, L	Hard Reset Configuration output. Driven during Hard Reset to the daughter board to signal the MPC that it should sample Hard Reset configuration from the data bus.
87	GND	GND	GND	GND		
88	R_PORI~	R_PORI~	R_PORI~	R_PORI~	O, L	Main battery power-on reset. Generated as a result of main 3.3V bus going through power up or power-down. Drives on-board logic as well either HARD-RESET or Power-On reset to the MPC.
89	GND	GND	GND	GND		
90						
91						

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TABLE 5-10. PM2 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
92	BWAITA~	BWAITA~	BWAITA~	BWAITA~	O, L	Buffered PCMCIA slot A WAIT signal. Used to prolong cycles to slow PC-Cards. In case of MPC823 or MPC850 daughter boards, connected to WAIT_B~ signal of the MPC.
93	GND	GND	GND	GND		
94	BWP	BWP	BWP	BWP	O, H	Buffered PCMCIA slot A Write Protect. In fact IP_A2/ IOIS16A~. Used as PC-card write protect indication or as 16 bit I/O capability indication for PCMCIA slot A. In case of MPC823 or MPC850 daughter boards, connected to IP_B2 signal of the MPC.
95	GND	GND	GND	GND		
96	BVS1	BVS1	BVS1	BVS1	O,X	Buffered PCMCIA slot A Voltage Sense 1. In fact IP_A0. Used in conjunction with BVS2 to determine the operation voltage of a PCMCIA card.
97	GND	GND	GND	GND		
98	BRDY	BRDY	BRDY	BRDY	O, H	Buffered PCMCIA slot A Ready signal. In fact IP_A7. Used as PCMCIA port A Card Ready indication.
99	GND	GND	GND	GND		
100						
101						
102	DP3	DP3	DP3	DP3	I/O, X	DP3/IRQ6~. Data Parity line 3 or Interrupt Request 6. May generate and receive parity data for D(24:31) bits connected to the DRAM SIMM. May also be configured as IRQ6~ input for the MPC.
103	GND	GND	GND	GND		
104	BVS2	BVS2	BVS2	BVS2	O, X	Buffered PCMCIA slot A Voltage Sense 2. In fact IP_A1. Used in conjunction with BVS1 to determine the operation voltage of a PCMCIA card.
105	GND	GND	GND	GND		
106	BCD1~	BCD1~	BCD1~	BCD1~	O, L	Buffered PCMCIA slot A Card Detect 1. In fact IP_A4. Input Port 4 of PCMCIA slot A. Used as Card Detect indication in conjunction with BCD2~.
107	GND	GND	GND	GND		

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TABLE 5-10. PM2 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
108	MODIN	MODIN	MODIN	MODIN	O, X	This signal selects between clock generator and the 32768 Hz crystal as clock sources for the MPC. Its is driven by DS2/4. See 2•3•2 "Clock Source Selection "on page 7. In the motherboard documentations.
109	GND	GND	GND	GND		
110	BBVD1	BBVD1	BBVD1	BBVD1	O, X	Buffered PCMCIA slot A Battery Voltage Detect 1. In fact IP_A6. Used in conjunction with BBVD2 to determine the battery status of a PC-Card.
111	GND	GND	GND	GND		
112	BCD2~	BCD2~	BCD2~	BCD2~	O, L	Buffered PCMCIA slot A Card Detect 2. In fact IP_A3. Input Port 3 of PCMCIA slot A. Used as Card Detect indication in conjunction with BCD1~.
113	GND	GND	GND	GND		
114	BBVD2	BBVD2	BBVD2	BBVD2	O, X	Buffered PCMCIA slot A Battery Voltage Detect 2. In fact IP_A5. Used in conjunction with BBVD1 to determine the battery status of a PC-Card.
115	GND	GND	GND	GND		
116						
117	N.C.	N.C.	N.C.	N.C.		
118	DP0	DP0	DP0	DP0	I/O	DP0/IRQ3~. Data Parity line 0 or Interrupt Request 3. May generate and receive parity data for D(0:7) bits connected to the DRAM SIMM. May not be configured as IRQ3~.
119	V3.3	V3.3	V3.3	V3.3		
120	DP2	DP2	DP2	DP2	I/O	DP2/IRQ5~. Data Parity line 2 or Interrupt Request 5. May generate and receive parity data for D(16:23) bits connected to the DRAM SIMM. May not be configured as IRQ5~.
121	V3.3	V3.3	V3.3	V3.3		
122	DP1	DP1	DP1	DP1	I/O	DP1/IRQ4~. Data Parity line1 or Interrupt Request 4. May generate and receive parity data for D(8:15) bits connected to the DRAM SIMM. May not be configured as IRQ4~.
123	V3.3	V3.3	V3.3	V3.3		
124	N.C.	N.C.	N.C.	N.C.		
125	V3.3	V3.3	V3.3	V3.3		

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TABLE 5-10. PM2 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
126	IRQ1~	IRQ1~	IRQ1~	IRQ1~	I/O, L	Interrupt Request 1.Pulled-up but otherwise not used on the FADS.
127	V3.3	V3.3	V3.3	V3.3		
128	SPARE3	SPARE3	MIITXEN	SPARE3	I/O, X	MPC's spare line 3. Pulled - up but otherwise unused on the FADS. This pin is used in MPC860T only as a MIITXEN signal for the Fast Ethernet.
129	V3.3	V3.3	V3.3	V3.3		
130	NC	NC	NC	NC		
131	V3.3	V3.3	V3.3	V3.3		
132	N.C.	N.C.	N.C.	N.C.		
133	V3.3	V3.3	V3.3	V3.3		
134	NMI~	NMI~	NMI~	NMI~	I/O, L	Non-Makable Interrupt. In fact IRQ0~ of the MPC. Driven by on-board logic by O.D. gate. Pulled - up. May be driven off-board by O.D. gate only.
135	V3.3	V3.3	V3.3	V3.3		
136	N.C.	N.C.	N.C.	N.C.		
137	V3.3	V3.3	V3.3	V3.3		
138	N.C.	N.C.	N.C.	N.C.		
139	V3.3	V3.3	V3.3	V3.3		
140	N.C.	N.C.	N.C.	N.C.		

a. Be aware that TRST~ is connected to GND with a zero ohm resistor.

TABLE 5-11. PM3 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
1	ETHRX	ETHRX	ETHRX	ETHRX	O, X	Ethernet port Receive Data. When the ethernet port is disabled via BCSR1 - tri-stated. Appears also at P8.
2	GND	GND	GND	GND		
3						
4	UUFEN~		UUFEN~		O, L	When this signal is active (LOW) it enable the LXT970 device. This signal connected to the TRSTE signal of the LXT970. In DTE mode when this pin is high the LXT970 isolate it self from the MII data interface. In repeater mode when it is high the LXT970 tree state the MII output pins.
5	ETHTX	ETHTX	ETHTX	ETHTX	I, X	Ethernet Port Transmit Data. Appears also at P8.
6	GND	GND	GND	GND		
7						
8	PC9	PC9	PC9	PC9	X, X	MPC's PI/O C 9 pin. Appears also at P8 but otherwise unused on the FADS.
9	IRDRXD	IRDRXD	IRDRXD	IRDRXD	O, X	InfraRed Port Receive Data. When the I/R port is disabled via BCSR1 - tri-stated. Appears also at P8.
10	GND	GND	GND	GND		
11	IRDTXD	IRDTXD	IRDTXD	IRDTXD	I, X	InfraRed Port Transmit Data. Appears also at P8.
12	GND	GND	GND	GND		
13						
14	PC8	PC8	PC8	PC8	I/O, X	MPC PI/O port C 8. Appears also at P8 but otherwise unused.
15	PA11	PA11	PA11	PA11	I/O, X	MPC PI/O port A 11. Appears also at P8 but otherwise unused.
16	GND	GND	GND	GND		
17	PA10	PA10	PA10	PA10	I/O, X	MPC PI/O port A 10. Appears also at P8 but otherwise unused.
18	GND	GND	GND	GND		
19						
20	PC7	PC7	PC7	PC7	I/O, X	MPC PI/O port C 7. Appears also at P8 but otherwise unused.

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TABLE 5-11. PM3 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
21	PA9	PA9	PA9	PA9	I/O, X	MPC PI/O port A 9. Appears also at P8 but otherwise unused.
22	GND	GND	GND	GND		
23	PA8	PA8	PA8	PA8	I/O, X	MPC PI/O port A 9. Appears also at P8 but otherwise unused.
24	GND	GND	GND	GND		
25						
26	PC13	PC13	PC13	PC13	I/O, X	MPC PI/O port C 13. Appears also at P8 but otherwise unused.
27	ETHTCK	ETHTCK	ETHTCK	ETHTCK	O, X	Ethernet port Transmit Clock. When the ethernet port is disabled via BCSR1 - tri-stated. Appears also at P8.
28	GND	GND	GND	GND		
29	ETHRCK	ETHRCK	ETHRCK	ETHRCK	O, X	Ethernet port Receive Clock. When the ethernet port is disabled via BCSR1 - tri-stated. Appears also at P8.
30	GND	GND	GND	GND		
31						
32	FETHCFG0		FETHCFG0		O, X	Fast Ethernet CFG0 signal When the LXT970 is in auto negotiation a low to high transition in this pin cause an auto negotiate to re-start. When auto negotiation is disabled this input selects operating speed bit 0.13 When this pin is high the 100Mbps is selected 0.13 = 1. When this pin is low the 10Mbps is selected 0.13 = 0.
33	PB31	PB31	PB31	PB31	I/O, X	MPC PI/O port B 31. Appears also at P8 but otherwise unused.
34	BINPAK~	BINPAK~	BINPAK~	RxCav	I/O	PCMCIA port Input Port Acknowledge. In fact PC15/ DREQ1~/RTS1~/L1ST1. When the PCMCIA port is disabled via BCSR1, may be used off-board for any alternate function. This Signal is used in the 860SAR as a RxCav signal this signal is one of the utopia bus signal.
35	PB30	PB30	PB30	PB30	I/O, X	MPC PI/O port B30. Appears also at P8 but otherwise unused.
36	GND	GND	GND	GND		
37	PB29	PB29	PB29	PB29	I/O, X	MPC PI/O port B 29. Appears also at P8 but otherwise unused.
38	RSTXD1	RSTXD1	RSTXD1	RSTXD1	I, X	RS232 Port 1 Transmit Data. When RS232 port 1 is disabled via BCSR1, may be used for any alternate function. Appears also at P8.

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TABLE 5-11. PM3 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
39	RSRXD1	RSRXD1	RSRXD1	RSRXD1	O, X	RS232 Port 1 Receive Data. When RS232 port 1 is disabled via BCSR1 - tri-stated and may be used for any alternate function. Appears also at P8.
40	RSDTR1~	RSDTR1~	RSDTR1~	RSDTR1~	O, L	RS232 port 1 DTR~ signal. When RS232 port 1 is disabled via BCSR1 - tri-stated and may be used for any alternate function. Appears also at P8.
41	GND	GND	GND	GND		
42	RSTXD2	RSTXD2	RSTXD2	PHSEL[1]	I, X	RS232 Port 2 Transmit Data. When RS232 port 2 is disabled via BCSR1, may be used for any alternate function. Appears also at P8. **(860SAR)** PHSEL[1]- Least significant bit of phy select bus (used for MPHY mod only)
43	RSRXD2	RSRXD2	RSRXD2	PHSEL[0]	O, X	RS232 Port 2 Receive Data. When RS232 port 2 is disabled via BCSR1 - tri-stated and may be used for any alternate function. Appears also at P8. **(860SAR)** PHSEL[0]- Least significant bit of phy select bus (used for MPHY mod only)
44	RSDTR2~	RSDTR2~	RSDTR2~	RSDTR2~	O, L	RS232 port 2 DTR~ signal. When RS232 port 2 is disabled via BCSR1 - tri-stated and may be used for any alternate function. Appears also at P8.
45	PC14	PC14	PC14	PC14	I/O, X	MPC PI/O port C 14. Appears also at P8 but otherwise unused.
46	GND	GND	GND	GND		
47	N.C.	N.C.	N.C.	N.C.		
48	GND	GND	GND	GND		
49						
50	PB27	PB27	PB27	PB27	I/O, X	MPC PI/O port B 27. Appears also at P8 but otherwise unused.
51	PB28	PB28	PB28	PB28	I/O, X	MPC PI/O port B 28. Appears also at P8 but otherwise unused.
52	GND	GND	GND	GND		
53	PC12	PC12	PC12	PC12	I/O, X	MPC PI/O port C 12. Appears also at P8 but otherwise unused.
54	PB26	PB26	PB26	PB26	I/O, X	MPC PI/O port C 26. Appears also at P8 but otherwise unused.
55	GND	GND	GND	GND		
56						

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TABLE 5-11. PM3 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
57	PA5	PA5	PA5	PA5	I/O, X	MPC PI/O port A 5. Appears also at P8 but otherwise unused.
58	GND	GND	GND	GND		
59						
60	PA4	PA4	PA4	PA4	I/O, X	MPC PI/O port A 4. Appears also at P8 but otherwise unused.
61	E_CLSN	E_CLSN	E_CLSN	E_CLSN	I/O, H	Ethernet Port Collision indication signal. Connected to the SCC's CTS~ signal. When the ethernet port is disabled via BCSR1, may be used off-board for any alternate function.
62	E_RENA	E_RENA	E_RENA	E_RENA	I/O, H	Ethernet Receive Enable. Connected to the SCC's CD~ signal. Active when there is network activity. When the ethernet port is disabled via BCSR1, may be used off-board for any alternate function.
63	SPARE2	SPARE2	MIIDIO	SPARE2	I/O, X	MPC spare line 2. Pulled - up but otherwise unused on the FADS. **(860T)** Transfer control information between the phy and mac.
64						Applies only for MPC823 daughter board. Video Encoder Enable Indication. Generated by BCSR4.
65	GND	GND	GND	GND		
66						
67	SYSCLK	SYSCLK	SYSCLK	SYSCLK	I, X	System Clock. In fact the CLKOUT of the MPC.
68	GND	GND	GND	GND		
69						
70						
71	PA3	PA3	PA3	PA3	I/O, X	MPC PI/O port A 3. Appears also at P8 but otherwise unused.
72	GND	GND	GND	GND		
73						
74	PA2	PA2	PA2	PA2	I/O, X	MPC PI/O port A 2. Appears also at P8 but otherwise unused.
75	PB17	PB17	PB17	PHREQ[1]	I/O, X	MPC PI/O port B 17. Appears also at P8 but otherwise unused. **(860T)** PHREQ[1] - least significant bit of phy request bus (used in PHY only)

TABLE 5-11. PM3 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
76	PB18	PB18	PB18	PB18	I/O, X	MPC PI/O port B 18. Appears also at P8 but otherwise unused.
77	E_TENA	E_TENA	E_TENA	E_TENA	I/O, H	Ethernet port Transmit Enable. Connected to the SCC's RTS~ signal. When active, transmit is enabled via the MC68160 EEST. When the ethernet port is disabled via BCSR1, may be used off-board for any alternate function.
78	GND	GND	GND	GND		
79	N.C.	N.C.	N.C.	N.C.		
80						
81						
82	ETHEN~	ETHEN~	ETHEN~	ETHEN~	O, L	Ethernet Port Enable. Connected to BCSR1. See TABLE 4-10. "BCSR1 Description" on page 49. In the motherboard documentations.
83	N.C.	N.C.	N.C.	N.C.		
84	IRD_EN~	IRD_EN~	IRD_EN~	IRD_EN~	O, L	Infra-Red Enable. Connected to BCSR1. See TABLE 4-10. "BCSR1 Description" on page 49.In the motherboard documentations.
85	PA1	PA1	PA1	PA1	I/O, X	MPC PI/O port A 1. Appears also at P8 but otherwise unused.
86	GND	GND	GND	GND		
87						
88	N.C.	N.C.	N.C.	N.C.		
89	PA0	PA0	PA0	PA0	I/O, X	MPC PI/O port A 0. Appears also at P8 but otherwise unused.
90	GND	GND	GND	GND		
91						
92	TMS	TMS	TMS	TMS	I/O, X	JTAG port Test Mode Select input. Used to select test through the JTAG port. Pulled-up but otherwise not used on the FADS.
93	PB16	PB16	PB16	PHREQ[0]	I/O, X	MPC PI/O port B 16. Appears also at P8 but otherwise unused. **(860T)** PHREQ[0] - least significant bit of phy request bus (used in PHY only)
94	TRST~	TRST~	TRST~	TRST~	O, L	JTAG port Reset. Pulled down with a zero ohm resistor, so that the JTAG logic is constantly reset. Otherwise unused on the FADS.

TABLE 5-11. PM3 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
95	PB15	PB15	PB15	PB15	I/O, X	MPC PI/O port B 15. Appears also at P8 but otherwise unused.
96	RS_EN1~	RS_EN1~	RS_EN1~	RS_EN1~	O, L	RS232 port 1 Enable. Connected to BCSR1. See TABLE 4-10. "BCSR1 Description" on page 49. In the motherboard documentations.
97	PB14	PB14	PB14	PB14	I/O, X	MPC PI/O port B 14. Appears also at P8 but otherwise unused.
98	PC4	PC4	PC4	PC4	I/O, X	MPC PI/O port C 4. Appears also at P8 but otherwise unused.
99	PC5	PC5	PC5	PC5	I/O, X	MPC PI/O port C 5. Appears also at P8 but otherwise unused.
100	PC6	PC6	PC6	PC6	I/O, X	MPC PI/O port C 6. Appears also at P8 but otherwise unused.
101	GND	GND	GND	GND		
102	RS_EN2~	RS_EN2~	RS_EN2~	RS_EN2~	O, L	RS232 port 1 Enable. Connected to BCSR1. See TABLE 4-10. "BCSR1 Description" on page 49. In the motherboard documentation.
103	SHIFT_C	**PD3**	MIITXD1	SOC	I/O, X	MPC860 PD3/RRJECT4~. MPC860T MIITXD1 is one of the Fast Ethernet MII Bus Pins MPC860SAR is the SOC pin one of the Utopia Bus.
104	GND	GND	GND	GND		
105						
106	HSYNC	**PD4**	MIITXD2	UTPB7	I/O, X	MPC860 PD4/RRJECT3~. MPC860T MIITXD2 is one of the Fast Ethernet MII Bus Pins MPC860SAR is the UTPB7 pin one of the Utopia Bus. Appears also at P8.
107	VSYNC	**PD5**	MIITXD3	UTPB6	I/O, X	MPC860 PD5/RRJECT2~. MPC860T MIITXD3 is one of the Fast Ethernet MII Bus Pins MPC860SAR is the UTPB6 pin one of the Utopia Bus. Appears also at P8.
108	GND	GND	GND	GND		
109						
110	LOE	**PD6**	MIIRXDV	UTPB5	I/O, X	MPC860 PD6/RRJECT3~. MPC860T MIITXRXDV is one of the Fast Ethernet MII Bus Pins MPC860SAR is the UTPB5 pin one of the Utopia Bus. Appears also at P8.

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TABLE 5-11. PM3 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
111	FETHRST~		FETHRST~		O, L	Fast Ethernet Reset. When this pin active (LOW) signal is being asserted the Fast ethernet tranceiver is being reset.
112	FETHCFG1		FETHCFG1		O, H	Fast Ethernet CFG1 signal When the LXT970 is in auto negotiation this pin determines operating speed advertisement capability in combination with MF4. see See the LXT970 documentation. When auto negotiation is disabled this input enables 10Mbps link test function and directly affects bit 19.8. When this pin is high, 10Mbps link test is disabled 19.8 = 1. When this pin is low, 10Mbps link test is enabled 19.8 = 0.
113	LD0	**PD7**	MIIRXER	UTPB4	I/O, X	MPC860s' PD7/RTS3~. MPC860T MIIRXER is one of the Fast Ethernet MII Bus Pins MPC860SAR is the UTPB4 pin one of the Utopia Bus. Appears also at P8.
114	LD1	**PD8**	MIIRXCLK			MPC860s' PD8/TXD4. MPC860T MIIRXCLK is one of the Fast Ethernet MII Bus Pins Bus.
115	LD2	**PD9**	MIITXD0	UTPCLK	I/O, X	MPC860s' PD9/RXD4. MPC860T MIITXD0 is one of the Fast Ethernet MII Bus Pins MPC860SAR is the UTPB7 pin one of the Utopia Bus.
116	LD3	**PD10**	MIIRXD0	TXENB	I/O, X	MPC860s' PD10/TXD3. MPC860T MIIRXD0 is one of the Fast Ethernet MII Bus Pins MPC860SAR is the TXENB pin one of the Utopia Bus. Appears also at P8.
117	LD4	**PD11**	MIITXER	RXENB	I/O, X	MPC860 PD11/RXD3. MPC860T MIITXER is one of the Fast Ethernet MII Bus Pins MPC860SAR is the RXENB pin one of the Utopia Bus. Appears also at P8.
118	LD5	**PD12**	MIIMDC	UTPB3	I/O	MPC860 PD12/L1RSYNCB. MPC860T MIIMDC is one of the Fast Ethernet MII Bus Pins MPC860SAR is the UTPB3 pin one of the Utopia Bus. Appears also at P8. Appears also at P8.

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TABLE 5-11. PM3 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
119	LD6	**PD13**	MIIRXD1	UTPB2	I/O, X	MPC860s' PD13/L1TSYNCB. MPC860T MIIRXD1 is one of the Fast Ethernet MII Bus Pins MPC860SAR is the UTPB2 pin one of the Utopia Bus. Appears also at P8.
120	LD7	**PD14**	MIIRXD2	UTPB1	I/O, X	MPC860 PD14/L1RSYNCA. MPC860T MIIRXD2 is one of the Fast Ethernet MII Bus Pins MPC860SAR is the UTPB1 pin one of the Utopia Bus. Appears also at P8.
121	LD8	**PD15**	MIIRXD3S	UTPB0	I/O, X	MPC860 PD15/L1TSYNCA. MPC860T MIIRXD3 is one of the Fast Ethernet MII Bus Pins MPC860SAR is the UTPB0 pin one of the Utopia Bus. Appears also at P8.
122	GND	GND	GND	GND		
123						
124	ETHLOOP	ETHLOOP	ETHLOOP	ETHLOOP	O, H	Ethernet Transceiver Diagnostic Loop-Back Control. Generated by BCSR4. See TABLE 4-23. "BCSR4 Description" on page 57. In the motherboard documentations.
125	TPFLDL~	TPFLDL~	TPFLDL~	TPFLDL~	O, L	Twisted Pair Full Duplex. Allows for full-duplex operation over the Ethernet Twisted-Pair channel. See TABLE 4-23. "BCSR4 Description" on page 57. In the motherboard documentations.
126	TPSQEL~	TPSQEL~	TPSQEL~	TPSQEL~	O, L	Twisted Pair Signal Quality Error Test Enable. See TABLE 4-23. "BCSR4 Description" on page 57. In the motherboard documentations.
127	MDM_AUD~	MDM_AUD~	MDM_AUD~	MDM_AUD~	O, L	Not used.
128	MODEMEN~	MODEMEN~	MODEMEN~	MODEMEN~	O, L	Not used.
129	N.C.	N.C.	N.C.	N.C.		
130	GND	GND	GND	GND		
131	N.C.	N.C.	N.C.	N.C.		
132						

TABLE 5-11. PM3 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
133	VCC	VCC	VCC	VCC		
134						
135						
136						
137						
138						
139						
140						

TABLE 5-12. PM4 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
1	GND	GND	GND	GND		
2	D31	D31	D31	D31	I/O, X	MPC's Data line 31.
3	GND	GND	GND	GND		
4	D30	D30	D30	D30	I/O, X	MPC's Data line 30.
5	GND	GND	GND	GND		
6	D29	D29	D29	D29	I/O, X	MPC's Data line 29.
7	GND	GND	GND	GND		
8	D28	D28	D28	D28	I/O, X	MPC's Data line28.
9	GND	GND	GND	GND		
10						
11						
12	D27	D27	D27	D27	I/O, X	MPC's Data line 27.
13	GND	GND	GND	GND		
14	D26	D26	D26	D26	I/O, X	MPC's Data line 26.
15	GND	GND	GND	GND		
16	D25	D25	D25	D25	I/O, X	MPC's Data line 25.
17	GND	GND	GND	GND		
18	D24	D24	D24	D24	I/O, X	MPC's Data line 24.
19	GND	GND	GND	GND		
20						
21						
22	D23	D23	D23	D23	I/O, X	MPC's Data line 23.
23	GND	GND	GND	GND		
24	D22	D22	D22	D22	I/O, X	MPC's Data line 22.
25	GND	GND	GND	GND		
26	D21	D21	D21	D21	I/O, X	MPC's Data line 21.
27	GND	GND	GND	GND		
28	D20	D20	D20	D20	I/O, X	MPC's Data line 20.

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TABLE 5-12. PM4 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
29	GND	GND	GND	GND		
30						
31						
32	D19	D19	D19	D19	I/O, X	MPC's Data line 191.
33	GND	GND	GND	GND		
34	D18	D18	D18	D18	I/O, X	MPC's Data line 18.
35	GND	GND	GND	GND		
36	D17	D17	D17	D17	I/O, X	MPC's Data line 17.
37	GND	GND	GND	GND		
38	D16	D16	D16	D16	I/O, X	MPC's Data line 16.
39	GND	GND	GND	GND		
40						
41						
42	D15	D15	D15	D15	I/O, X	MPC's Data line 15.
43	GND	GND	GND	GND		
44	D14	D14	D14	D14	I/O, X	MPC's Data line 14.
45	GND	GND	GND	GND		
46	D13	D13	D13	D13	I/O, X	MPC's Data line 13.
47	GND	GND	GND	GND		
48	D12	D12	D12	D12	I/O, X	MPC's Data line 12.
49	GND	GND	GND	GND		
50						
51						
52	D11	D11	D11	D11	I/O, X	MPC's Data line 11.
53	GND	GND	GND	GND		
54	D10	D10	D10	D10	I/O, X	MPC's Data line 10.
55	GND	GND	GND	GND		
56	D9	D9	D9	D9	I/O, X	MPC's Data line 9.
57	GND	GND	GND	GND		
58	D8	D8	D8	D8	I/O, X	MPC's Data line 8.

TABLE 5-12. PM4 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
59	GND	GND	GND	GND		
60						
61						
62	D7	D7	D7	D7	I/O, X	MPC's Data line 7.
63	GND	GND	GND	GND		
64	D6	D6	D6	D6	I/O, X	MPC's Data line 6.
65	GND	GND	GND	GND		
66	D5	D5	D5	D5	I/O, X	MPC's Data line 5.
67	GND	GND	GND	GND		
68	D4	D4	D4	D4	I/O, X	MPC's Data line 4.
69	GND	GND	GND	GND		
70						
71						
72	D3	D3	D3	D3	I/O, X	MPC's Data line 3.
73	GND	GND	GND	GND		
74	D2	D2	D2	D2	I/O, X	MPC's Data line 2.
75	GND	GND	GND	GND		
76	D1	D1	D1	D1	I/O, X	MPC's Data line 1.
77	GND	GND	GND	GND		
78	D0	D0	D0	D0	I/O, X	MPC's Data line 0.
79	GND	GND	GND	GND		
80						
81	DRMH_W~	DRMH_W~	DRMH_W~	DRMH_W~	O, L	Dram Half Word. Sets the Dram to 16 bit data bus width. See TABLE 4-10. "BCSR1 Description" on page 49. In the motherboard documentations.
82	DRAMEN~	DRAMEN~	DRAMEN~	DRAMEN~	O, L	Dram Enable. Enables Dram to the FADS memory map. See TABLE 4-10. "BCSR1 Description" on page 49. In the motherboard documentations.
83	FCFGEN~	FCFGEN~	FCFGEN~	FCFGEN~	O, L	Flash Configuration Enable. Allows for Hard Reset Configuration to be obtained from the Flash memory provided that this option is supported by the MPC. See TABLE 4-10. "BCSR1 Description" on page 49. In the motherboard documentations.

TABLE 5-12. PM4 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
84	F_EN~	F_EN~	F_EN~	F_EN~	O, L	Flash Enable. Enables the Flash memory to the FADS memory map. See TABLE 4-10. "BCSR1 Description" on page 49 In the motherboard documentations.
85	SDRAMEN	SDRAMEN	SDRAMEN	SDRAMEN	O, H	Sdram Enable. Enables the Synchronous Dram to the FADS memory map. See TABLE 4-10. "BCSR1 Description" on page 49. In the motherboard documentations.
86	BCSREN~	BCSREN~	BCSREN~	BCSREN~	O, L	BCSR Enable. Enables the BCSR to the FADS memory map. See TABLE 4-10. "BCSR1 Description" on page 49. In the motherboard documentations.
87	FETHFDE	FETHFDE	FETHFDE	FETHFDE	O, X	Full Duplex Enable when auto negotiation is enable the FDE pin of the LXT970 determine full duplex advertisement capability in combination with MF4 and CFG1. See than LXT970 documentation. When auto negotiation is disable the FDE pin of the LXT970 effects full duplex and determines the value of bit 0.8 Duplex Mode. When this pin is high Full Duplex in Enable. 0.8 = 1. When this pin is low Full Duplex is Disable 0.8 = 0.
88	PCCEN~	PCCEN~	PCCEN~	PCCEN~	O, L	PC- Card Enable. Enables the PC-Card to be accessed by the FADS.
89	EXTOLI0	EXTOLI0	EXTOLI0	EXTOLI0	I/O, X	External Tool Identification 0. Connected to BCSR2. See 4•11•4 "BCSR2 - Board Control / Status Register - 2" on page 51.In the motherboard documentations.
90	SGLAMP~	SGLAMP~	SGLAMP~	SGLAMP~	O, L	Signaling Lamp. Used for misc. s/w signaling purpose. See TABLE 4-23. "BCSR4 Description" on page 57. In the motherboard documentations.
91	EXTOLI2	EXTOLI2	EXTOLI2	EXTOLI2	I/O, X	External Tool Identification 2. Connected to BCSR2. See 4•11•4 "BCSR2 - Board Control / Status Register - 2" on page 51.In the motherboard documentations.
92	USBVCC1	USBVCC1	USBVCC1	USBVCC1	O, X	Applies only for MPC823DB. Reserved Signal for USB Power. See TABLE 4-23. "BCSR4 Description" on page 57. In the motherboard documentations.
93	DBREV0	DBREV0	DBREV0	DBREV0	I, X	Daughter Board Revision Code Signal 0. The MSB of the D/B revision Code. See TABLE 4-13. "BCSR2 Description" on page 52. In the motherboard documentations.
94	EXTOLI1	EXTOLI1	EXTOLI1	EXTOLI1	I/O, X	External Tool Identification 1. Connected to BCSR2. See 4•11•4 "BCSR2 - Board Control / Status Register - 2" on page 51. In the motherboard documentations.

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TABLE 5-12. PM4 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
95	DBREV2	DBREV2	DBREV2	DBREV2	I, X	Daughter Board Revision Code Signal 2. The LMSB of the D/B revision Code. See TABLE 4-13. "BCSR2 Description" on page 52. In the motherboard documentations.
96	EXTOLI3	EXTOLI3	EXTOLI3	EXTOLI3	I/O, X	External Tool Identification 3. Connected to BCSR2. See 4•11•4 "BCSR2 - Board Control / Status Register - 2" on page 51. In the motherboard documentations.
97	BCSR3R1	BCSR3R1	BCSR3R1	BCSR3R1	I/O, X	Reserved signal 1 in BCSR3. See TABLE 4-19. "BCSR3 Description" on page 55. In the motherboard documentations.
98	DBREV1	DBREV1	DBREV1	DBREV1	I/O, X	Daughter Board Revision Code Signal 1. See TABLE 4-13. "BCSR2 Description" on page 52. In the motherboard documentations.
99	DBID1	DBID1	DBID1	DBID1	I/O, X	Daughter Board ID Code 1. Part of the field which designates the type of daughter board connected. See TABLE 4-19. "BCSR3 Description" on page 55 In the motherboard documentations.
100	BCSR3R0	BCSR3R0	BCSR3R0	BCSR3R0	I/O, X	Reserved signal 0 in BCSR3. See TABLE 4-19. "BCSR3 Description" on page 55 In the motherboard documentations.
101	DBID3	DBID3	DBID3	DBID3	I/O, X	Daughter Board ID Code 3. Part of the field which designates the type of daughter board connected. See TABLE 4-19. "BCSR3 Description" on page 55 In the motherboard documentations.
102	DBID0	DBID0	DBID0	DBID0	I/O, X	Daughter Board ID Code 0. Part of the field which designates the type of daughter board connected. See TABLE 4-19. "BCSR3 Description" on page 55 In the motherboard documentations.
103	DBID5	DBID5	DBID5	DBID5	I/O, X	Daughter Board ID Code 5. Part of the field which designates the type of daughter board connected. See TABLE 4-19. "BCSR3 Description" on page 55 In the motherboard documentations.
104	DBID2	DBID2	DBID2	DBID2	I/O, X	Daughter Board ID Code 2. Part of the field which designates the type of daughter board connected. See TABLE 4-19. "BCSR3 Description" on page 55 In the motherboard documentations.
105	BCSR3R13	BCSR3R13	BCSR3R13	BCSR3R13	I/O, X	Reserved signal 13 in BCSR3. See TABLE 4-19. "BCSR3 Description" on page 55 In the motherboard documentations.

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TABLE 5-12. PM4 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
106	DBID4	DBID4	DBID4	DBID4	I/O, X	Daughter Board ID Code 4. Part of the field which designates the type of daughter board connected. See TABLE 4-19. "BCSR3 Description" on page 55 In the motherboard documentations.
107	CHINS~	CHINS~	CHINS~	CHINS~	I/O, L	Chip In Socket. When this signal is active (low), FADS logic is noticed that the evaluated MPC8XX resides in its socket. If inactive, either the MPC is out of socket or a daughter board is not connected, in which case the FADS becomes a debug station.
108	GND	GND	GND	GND		
109						
110	N.C.	N.C.	N.C.	N.C.		
111						
112	GND	GND	GND	GND		
113						
114	N.C.	N.C.	N.C.	N.C.		
115						
116	GND	GND	GND	GND		
117						
118	N.C.	N.C.	N.C.	N.C.		
119						
120	GND	GND	GND	GND		
121						
122	N.C.	N.C.	N.C.	N.C.		
123						
124	GND	GND	GND	GND		
125						
126	N.C.	N.C.	N.C.	N.C.		
127						
128	GND	GND	GND	GND		
129						
130	N.C.	N.C.	N.C.	N.C.		
131						

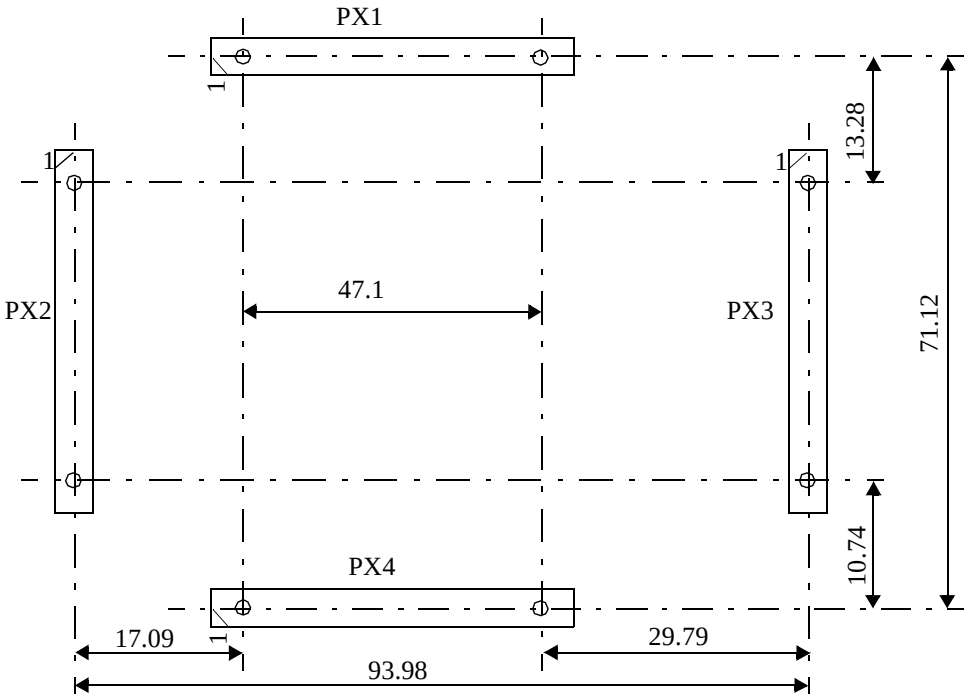
TABLE 5-12. PM4 Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***(General)***	*860 Daughter Signal Name*	*860T Daughter Signal Name*	*860SAR Daughter Signal Name*	*Attribute*	*Description*
132	GND	GND	GND	GND		
133						
134	N.C.	N.C.	N.C.	N.C.		
135						
136	GND	GND	GND	GND		
137						
138	N.C.	N.C.	N.C.	N.C.		
139						
140	GND	GND	GND	GND		

5•1•4 PX1 - PX4 Hardware Expansion Connectors

These connectors are receptacle inter-board connectors made by Molex. They are identical to those exist on the MPC8XXFADS mother board. Their mechanical assembly is similar as well and is shown in FIGURE 5-2 "Expansion Connectors Mechanical Assembly" below:

FIGURE 5-2 Expansion Connectors Mechanical Assembly



In principle, the expansion connectors are identical in signals assignment to the mother boards connectors. However, there is a difference mainly between PM3 and PX3, resulting from the difference between the various members of the 8XX family. Therefore, in the following tables only the differences are documented per each connector pair - PM1 - PX1...

TABLE 5-13. PX1 - PM1 Interconnect Signals' Differences

Pin No.	*Signal Name*	*Attribute*	*Description*
			No Difference

TABLE 5-14. PX2 - PM2 Interconnect Signals' Differences

Pin No.	*Signal Name*	*Attribute*	*Description*
76	EXTCLK	O, X	External Clock. 4MHz clock generator output, the input clock to the MPC.

TABLE 5-15. PX3 - PM3 Interconnect Signals' Differences

Pin No.	*Signal Name*	*Attribute*	*Description*
			No Difference

TABLE 5-16. PX4 - PM4 Interconnect Signals' Differences

Pin No.	*Signal Name*	*Attribute*	*Description*
			No Difference

5•1•5 MPC8XXFADS's P8 - Serial Ports' Expansion Connector

P8 is a 96 pin, 90º, DIN 41612 connector, which allows for convenient expansion of the MPC's serial ports. Although this connector resides on the mother board it is documented here, this, since it's signal assignment is unique per each MPC8XX. For the 860SAR this connector is the connector which through it the user will operate the 860SAR-PHY board. In the 860SAR-PHY board this connector called P13.

Note:

The contents of TABLE 5-17. "P8 - Interconnect Signals" below**, might conflict with MPC8XXFADS's schematic page 14. This since, that the schematic page is named in MPC821/860 terms. In such case, this table overrides!**

TABLE 5-17. P8 - Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***General***	*860 Daughter Board Signal Name*	*860T Daughter Board Signal Name*	*860Sar Daughter Board Signal Name*	*Attribute*	*Description*
A1	ETHRX	ETHRX	ETHRX	ETHRX	I/O	Ethernet port receive data. See PM3(1)
A2	ETHTX	ETHTX	ETHTX	ETHTX	I/O	Ethernet Port transmit data. See PM3(5,11,42)
A3	IRDRXD	IRDRXD	IRDRXD	IRDRXD	I/O	IrDA port receive data. See PM3(9).
A4	IRDTXD	IRDTXD	IRDTXD	IRDTXD	I/O	IrDA port transmit data. See PM3(5,11,42)
A5	LD4	PD11	MIITXER	RXENB	I/O	Also VD3. See PM3(117)
A6	LD3	PD10	MIIRXD0	TXENB	I/O	Also VD2. See PM3(116)
A7	LD2	PD9	MIITXD0	UTPCLK	I/O	Also VD1. See PM3(115)
A8	LD1	PD8	MIIRXCLK	UTPB[4]	I/O	Also VD0. See PM3(114)
A9	ETHTCK	ETHTCK	ETHTCK	ETHTCK	I/O	Ethernet port transmit clock. See PM3(27).
A10	ETHRCK	ETHRCK	ETHRCK	ETHRCK	I/O	Ethernet port receive clock. See PM3(29)
A11	PA5	PA5	PA5	L1TSYNCB (TIN2)	I/O	If the 860Sar is used with the 860Sar-phy board this signal can be use for L1TSYNCB.
A12	PA4	PA4	PA4	L1TCLKB (TOUT2)	I/O	BRGCLK2/$\overline{\text{TOUT2}}$/CLK4/**PA[4]**. See PM3(60) If the 860Sar is used with the 860Sar-phy board this signal can be use for L1TCLKB.
A13	PA3	PA3	PA3	PA3 (AD3)	I/O	If the 860Sar is used with the 860Sar-phy board this signal can be use for AD3 in the 860Sar-Phy Board.
A14	L1RCLKB	L1RCLKB	L1RCLKB	L1RCLKB	I/O	See PM3(74) If the 860Sar is used with the 860Sar-phy board this signal can be use for L1RCLKB in the 860Sar-Phy Board.
A15	PA1	PA1	PA1	PA1 (AD2)	I/O	If the 860Sar is used with the 860Sar-phy board this signal can be use for AD2 in the 860Sar-Phy Board.
A16	PA0	PA0	PA0	PA0 (L1TCLKB)	I/O	If the 860Sar is used with the 860Sar-phy board this signal can be use for L1TCLKB in the 860Sar-Phy Board.
A17	VCC	VCC	VCC	VCC	-	
A18	PA9	PA9	PA9	PA9 (L1TXDB)	I/O	See PM3(15,21). If the 860Sar is used with the 860Sar-phy board this signal can be use for L1TXDB in the 860Sar-Phy Board.
A19	L1RXDB	L1RXDB	L1RXDB	L1RXDB	I/O	See PM3(17). If the 860Sar is used with the 860Sar-phy board this signal can be use for L1RXDB in the 860Sar-Phy Board.

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TABLE 5-17. P8 - Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***General***	*860 Daughter Board Signal Name*	*860T Daughter Board Signal Name*	*860Sar Daughter Board Signal Name*	*Attribute*	*Description*
A20	PA9	PA9	PA9	PA9 (AD7)	I/O	See PM3(21). If the 860Sar is used with the 860Sar-phy board this signal can be use for AD7 in the 860Sar-Phy Board.
A21	L1RXDA	L1RXDA	L1RXDA	L1RXDA (AD6)	I/O	See PM3(23) If the 860Sar is used with the 860Sar-phy board this signal can be use for AD6 in the 860Sar-Phy Board.
A22	GND	GND	GND	GND	-	
A23	GND	GND	GND	GND	-	
A24	IRQ7~	IRQ7~	IRQ7~	IRQ7~	I, L	See PM2(130)
A25	FRZ	FRZ	FRZ	FRZ	I/O	See PM2(24).
A26	ETHEN~	ETHEN~	ETHEN~	ETHEN~	O	See PM3(82)
A27	IRQ3~.	IRQ3~	IRQ3~	IRQ3~	I/L	
A28	IRQ2~	IRQ2~	IRQ2~	IRQ2~	I, L	RSV/IRQ2~. See PM2(26). Used as an IRQ in the 860T Daughter Board and in the 860Sar-PHY Board.
A29	IRQ1~	IRQ1~	IRQ1~	IRQ1~	I, L	See PM2(126).
A30	NMI~	NMI~	NMI~	NMI~	I, L	See PM2(134).
A31	RS_EN1~	RS_EN1~	RS_EN1~	RS_EN1~	O,L	See PM3(96).
A32	GND	GND	GND	GND	-	
B1	LCD_A	PB31	PB31	PB31	I/O	LCD_A/PB31. See PM3(33).
B2	PB30	PB30	PB30	PB30 (SPI_CLK)	I/O	See PM3(35). If the 860Sar is used with the 860Sar-phy board this signal can be use for SPI_CLK in the 860Sar-Phy Board.
B3	PB29	PB29	PB29	PB29 (SPI_IN)	I/O	See PM3(37). If the 860Sar is used with the 860Sar-phy board this signal can be use for SPI_IN in the 860Sar-Phy Board.
B4	PB28	PB28	PB28	PB28 (SPI_OUT)	I/O	See PM3(51). If the 860Sar is used with the 860Sar-phy board this signal can be use for SPI_IN in the 860Sar-Phy Board.
B5	I2CDAT	PB27	PB27	PB27 (PC_PHY)	I/O	PB27/I2CDAT. See PM3(50). If the 860Sar is used with the 860Sar-phy board this signal can be use for CS_PHY in the 860Sar-Phy Board.

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TABLE 5-17. P8 - Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***General***	*860 Daughter Board Signal Name*	*860T Daughter Board Signal Name*	*860Sar Daughter Board Signal Name*	*Attribute*	*Description*
B6	PB26	PB26	PB26	PB26 (RST_BR)	I/O	PB26/I2CCLK. See PM3(54). If the 860Sar is used with the 860Sar-phy board this signal can be use for RST_BRD in the 860Sar-Phy Board.
B7	RSTXD1	RSTXD1	RSTXD1	RSTXD1	I/O	See PM3(38).
B8	RSRXD1	RSRXD1	RSRXD1	RSRXD1	I/O	See PM3(39).
B9	RSDTR1~	RSDTR1~	RSDTR1~	RSDTR1~	I/O	See PM3(40).
B10	RSDTR2~	RSDTR2~	RSDTR2~	RSDTR2~	I/O	See PM3(44).
B11	RSTXD2.	RSTXD2.	RSTXD2.	RSTXD2.	I/O	See PM3(5,11,42).
B12	RSRXD2	RSRXD2	RSRXD2	RSRXD2	I/O	See PM3(43)
B13	E_TENA	E_TENA	E_TENA	E_TENA	I/O	See PM3(77).
B14	LCD_B	PB18	PB18	PB18 (READ)	I/O	PB18/LCD_B. See PM3(76). If the 860Sar is used with the 860Sar-phy board this signal can be use for READ in the 860Sar-Phy Board.
B15	LCD_C	PB17	PB17	PB17 (AD5)	I/O	PB17/LCD_C. See PM3(75). If the 860Sar is used with the 860Sar-phy board this signal can be use for AD5 in the 860Sar-Phy Board.
B16	PB16	PB16	PB16	PB16 (AD4)S	I/O	See PM3(93). If the 860Sar is used with the 860Sar-phy board this signal can be use for AD4 in the 860Sar-Phy Board.
B17	PB15	PB15	PB15	PB15 (TCAV)	-	If the 860Sar is used with the 860Sar-phy board this signal can be use for TCAV in the 860Sar-Phy Board.
B18	PB14	PB14	PB14	PB14 (ALE)	-	If the 860Sar is used with the 860Sar-phy board this signal can be use for ALE in the 860Sar-Phy Board.
B19	GND	GND	GND	GND	-	
B20	BINPAK~	BINPAK~	BINPAK~	BINPAK~ (RCAV)	I/O	See PM3(34). If the 860Sar is used with the 860Sar-phy board this signal can be use for RCAV in the 860Sar-Phy Board.
B21	PC14	PC14	PC14	PC14 (LF~)	I/O	See PM3(45). If the 860Sar is used with the 860Sar-phy board this signal can be use for LF~ in the 860Sar-Phy Board.
B22	PC13	PC13	PC13	PC13 (CS_T1~)	I/O	See PM3(26). If the 860Sar is used with the 860Sar-phy board this signal can be use for CS_T1~S in the 860Sar-Phy Board.
B23	PC12	PC12	PC12	PC12	I/O	See PM3(53).

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TABLE 5-17. P8 - Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***General***	*860 Daughter Board Signal Name*	*860T Daughter Board Signal Name*	*860Sar Daughter Board Signal Name*	*Attribute*	*Description*
B24	E_CLSN	E_CLSN	E_CLSN	E_CLSNS	I/O	See PM3(61).
B25	E_RENA	E_RENA	E_RENA	E_RENA	I/O	See PM3(62).
B26	USBRXP	PC9	PC9	PC9 (AD1)	I/O	See PM3(8). If the 860Sar is used with the 860Sar-phy board this signal can be use for AD1 in the 860Sar-Phy Board.
B27	USBRXN	PC8	PC8	PC8 (AD0)	I/O	See PM3(14). If the 860Sar is used with the 860Sar-phy board this signal can be use for AD0 in the 860Sar-Phy Board.
B28	USBTXP	PC7	PC7	PC7 (L1RSYNCB)	I/O	See PM3(20). If the 860Sar is used with the 860Sar-phy board this signal can be use for L1TSYNCB in the 860Sar-Phy Board.
B29	L1RSYNCB	PC6	PC6	PC6 (L1RSYNCB)	I/O	See PM3(100). If the 860Sar is used with the 860Sar-phy board this signal can be use for L1RSYNCB in the 860Sar-Phy Board.
B30	PC5	PC5	PC5	PC5	I/O	See PM3(99).
B31	L1RSYNCA	PC4	PC4	PC4	I/O	See PM3(98).
B32	GND	GND	GND	GND	-	
C1	VCC	VCC	VCC	VCC		
C2						
C3						
C4						
C5						
C6	RS_EN2~	RS_EN2~	RS_EN2~	RS_EN2~	O, L	See PM3(102).
C7	GND	GND	GND	GND		
C8						
C9						
C10						
C11						
C12						
C13						
C14						

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TABLE 5-17. P8 - Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***General***	*860 Daughter Board Signal Name*	*860T Daughter Board Signal Name*	*860Sar Daughter Board Signal Name*	*Attribute*	*Description*
C15	VD7	PD15	MIIRXD3	PD15 (UTPB[0])	I/O	See PM3(121). If the 860Sar is used with the 860Sar-phy board this signal can be use for UTPB[0] in the 860Sar-Phy Board
C16	VD6	PD14	MIIRXD2	PD14 (UTPB[1])	I/O	See PM3(120). If the 860Sar is used with the 860Sar-phy board this signal can be use for UTPB[1] in the 860Sar-Phy Board
C17	VD5	PD13	MIIRXD1	PD13 (UTPB[2])	I/O	See PM3(119). If the 860Sar is used with the 860Sar-phy board this signal can be use for UTPB[2] in the 860Sar-Phy Board
C18	VD4	PD12	MIIMDC	PD12 (UTPB[3])	I/O	See PM3(118). If the 860Sar is used with the 860Sar-phy board this signal can be use for UTPB[3] in the 860Sar-Phy Board
C19	FIELD	PD7	MIIRXER	PD7 (UTPB[4])	I/O	See PM3(113). If the 860Sar is used with the 860Sar-phy board this signal can be use for UTPB[4] in the 860Sar-Phy Board
C20	BLANK~	PD6	MIIRXDV	PD6 (UTPB[5])	I/O	See PM3(110). If the 860Sar is used with the 860Sar-phy board this signal can be use for UTPB[5] in the 860Sar-Phy Board
C21	VCC	VCC	VCC	VCC	-	
C22	HRESET~	HRESET~	HRESET~	HRESET~	I/O, L	See PM2(84).
C23	SRESET~	SRESET~	SRESET~	SRESET~	I/O, L	See PM2(80).
C24	N.C.	N.C.	N.C.	N.C.	-	Not Connected
C25	VCC	VCC	VCC	VCC	-	
C26	VDOCLK	PD3	MIITXD1	PD3 (SOC)	I/O	See PM3(103) If the 860Sar is used with the 860Sar-phy board this signal can be use for SOC in the 860Sar-Phy Board
C27	VPPIN	VPPIN	VPPIN	VPPIN	I/O	+12V input for PCMCIA flash programming. Parallel to P7 of the MPC8XXFADS.
C28						
C29	GND	GND	GND	GND	-	
C30	HSYNC	PD4	MIITXD2	PD4 (UTPB[7])	I/O	See PM3(106). If the 860Sar is used with the 860Sar-phy board this signal can be use for UTPB[7] in the 860Sar-Phy Board

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TABLE 5-17. P8 - Interconnect Signals

Pin No.	*Daughter Board Signal Name* ***General***	*860 Daughter Board Signal Name*	*860T Daughter Board Signal Name*	*860Sar Daughter Board Signal Name*	*Attribute*	*Description*
C31	GND	GND	GND	GND	-	
C32	VSYNC	PD5	MIITXD3	PD5 (UTPB[6])	I/O	See PM3(107). If the 860Sar is used with the 860Sar-phy board this signal can be use for UTPB[6] in the 860Sar-Phy Board

5•2 MPC860TFADSDB Part List

In this section the MPC860TFADSDB bill of material is listed according to their reference designation.

TABLE 5-18. PILOT Part List

Reference Designation	*Part Description*	*Type*	*Part Number*	total
BOARD			084 00114	1
C5 C6 C7 C8 C9 C10 C11 C12 C14 C15 C16 C17 C19 C20 C22 C23 C24 C25 C28 C29 C32 C37 C38 C39 C40 C43 C47 C48 C49 C52 C53	Capacitor 0.1µF,16V, 10%, 0603, Ceramic	SMD	021 00118	31
C2 C3 C4 C31 C33 C34 C36 C51	Capacitor 10µF, 20V, 10%, Size C, Tantalum	SMD	023 00027	8
C13	Capacitor 100µF, 10V, 10%, Size D, Tantalum	SMD	023 00038	1
C30 C35	Capacitor 1µF, 25V, 10%, Size A, Tantalum	SMD	023 00028	2
C18 C21	Capacitor 10pF, 50V 10%, COG, 1206, Ceramic	SMD	021 00097	2
C26	Capacitor 5000pF, 50V, 10%, 1206, Ceramic	SMD	021 00080	1
C27	Capacitor 0.68µF, 20V, 10%, Size A, Tantalum	SMD	023 00041	1
C1 C44 C45 C46	Cap 0.01µF 50V 10% NPO 1206	SMD	021 00070	4
C41 C42	Cap 18pF 50V COG 1206 CER T/R	SMD	021 00128	2
C50	Cap 1nF2KV X7R 1210 CER CAP T/R	SMD	021 00126	1
D1	Diode SMD LL4004G	SMD	048 LL4004G	1
DS1	Dip Switch 90HBW08S	SMD	040 00027	1
H1 H2 H3	Gnd Bridge, Gold Plated	TH	022 00011	3
J1 J2 J3	Jumper Header, 3 Pole with Fabricated Jumper	TH	028 00162	3
J1 J2 J3		TH	009 00124	3
J4 J5	Jumper, Soldered.	TH	022 00011	2
L1	Inductor 8.2 mHy	TH	024 00020	1
L2 L3 L4 L5 L6 L7	Ferrite bid	SMD	024 00013	6
LD1 LD2 LD3 LD4 LD5 LD6 LD7	Led Green	SMD	048 01005	7
P1 P2 P3 P4 P5 P6 P8	Connector 38 pin, Receptacle MICTOR.	SMD	009 00393	7

Support Information

TABLE 5-18. PILOT Part List

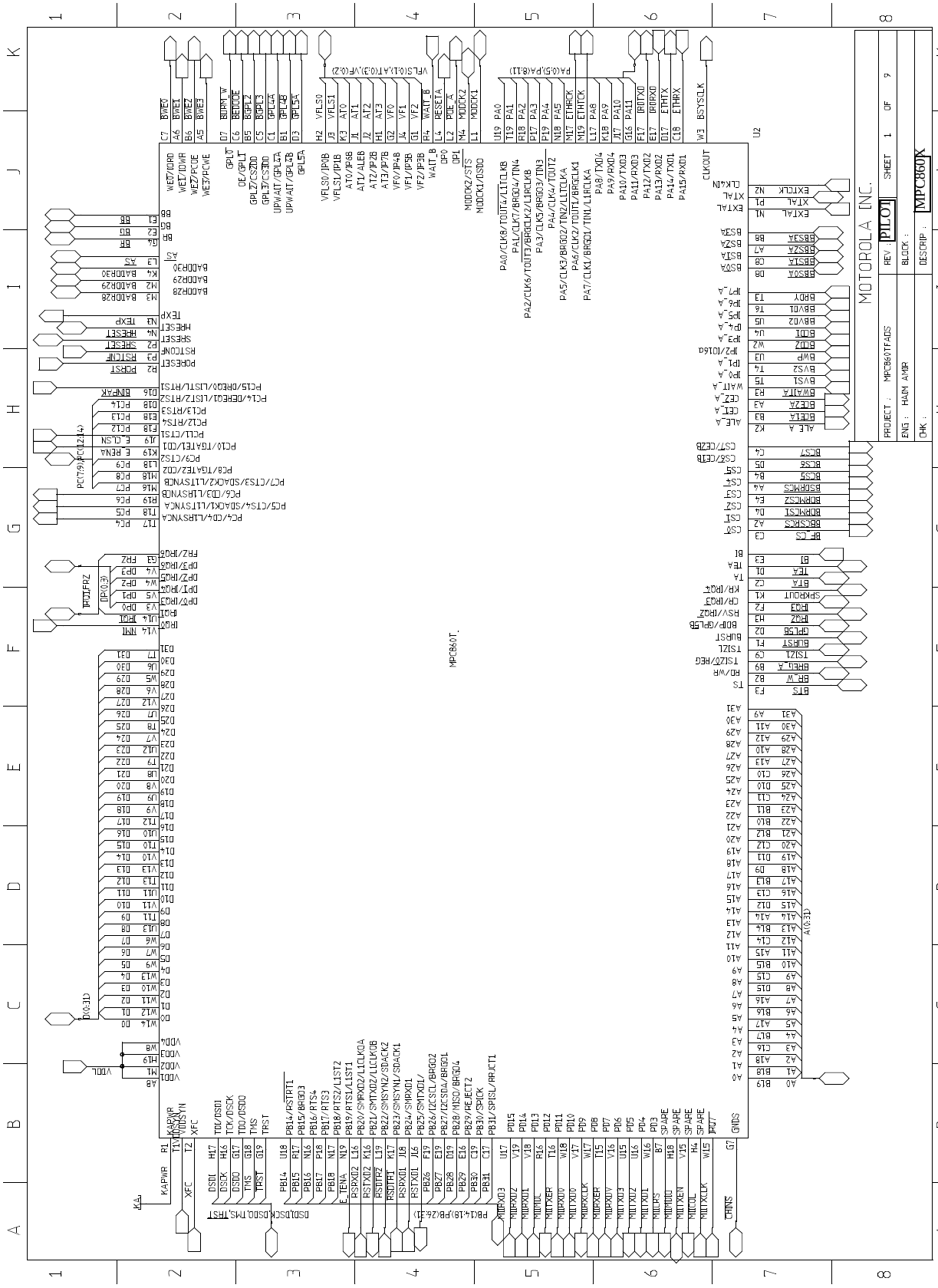
Reference Designation	*Part Description*	*Type*	*Part Number*	total
P9	RJ_45 8PIN CONNECTOR	TH	009 00236	1
P7	Connector Header, 40 pin, Dual In-line,TSM-115-04-S-DV	SMD	028 00165	1
PM1 PM2 PM3 PM4	Connector Inter-board, 7mm Height, 140 pin, Plug	SMD	028 00392	4
PX1 PX2 PX3 PX4	Connector Inter-board 140 pin, Receptacle	SMD	009 00172	4
R15 R17 R18 R21	22Ω,	SMD	006 00301	4
R25	Faire-Rite s/n 274309447	SMD	024 ???	1
R1 R2 R3 R4 R22 R23 R24 R26 R42 R43	55Ω, 1% /51.1Ω if ther is no 55Ω	SMD	006 00???	10
R45	Resistor 100 Ω, 1%, 1206, 1/8W	SMD	006 00240	1
R5 R6 R51 R52	Resistor 191 Ω, 1%, 1206, 1/8W	SMD	006 00344	4
R46 R55 R56 R57 R58 R63 R64 R65	Resistor 51.1Ω, 1%, 1206, 1/8W	SMD	006 00221	8
R8 R9 R10 R59 R60	Resistor 75 Ω, 5%, 1206, 1/ 8W	SMD	006 00260	5
R27	Resistor 4.7 KΩ, 5%, 1206, 1/8W	SMD	006 00254	1
R7 R37 R38 R39 R40 R41	Resistor 330 Ω, 5%, 1206, 1/8W	SMD	006 00237	6
R11	Resistor 47 KΩ, 1%, 1206, 1/8W	SMD	006 00261	1
R12	Resistor 200 KΩ, 5%, 1206, 1/8W	SMD	006 00298	1
R13	Resistor 20 MΩ, 5%, 1206, 1/8W	SMD	006 00314	1
R14 R16 R19 R20 R29 R31 R32 R33 R34 R35 R48 R49	Resistor 0 Ω, 1206, 1/8W	SMD	006 00252	12
R28 R30	0 (*) not use	SMD	006 00252	2
R36	Resistor 124 KΩ, 5%, SMD 1206, 1/ 8W	SMD	006 00299	1
R47 R50 R61 R62	Resistor 69.8 Ω, 1%, 1206, 1/8W	SMD	006 00345	4
R44	Resistor 22.1KΩ,1%, 1206, 1/8W	SMD	006 006 00236	1
R53	Resistor 243 Ω, 1%, 1206, 1/8W	SMD	006 006 00215	1
R54	Resistor 143 Ω, 5%, 1206, 1/8W	SMD	006 00300	1

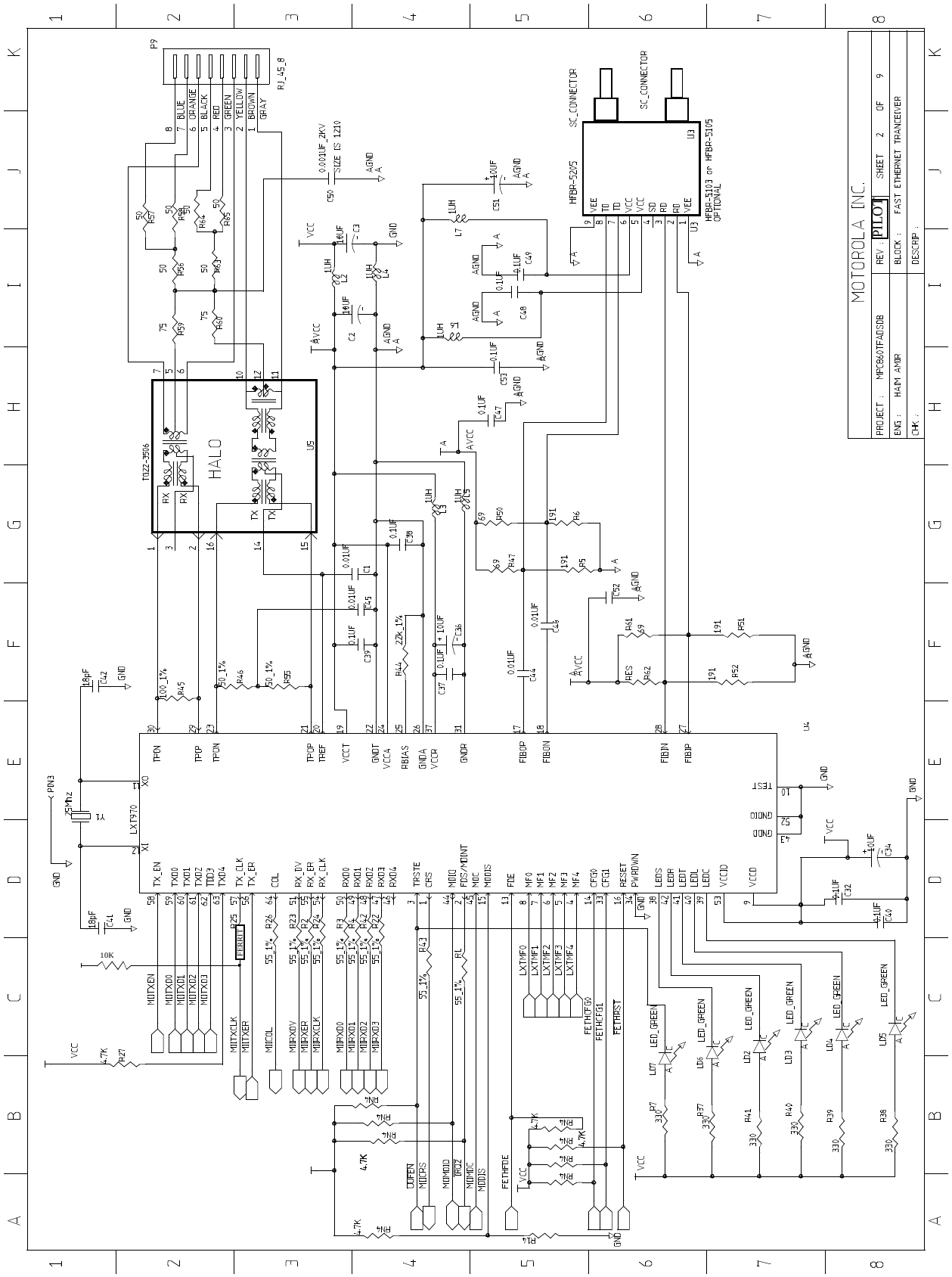
Support Information

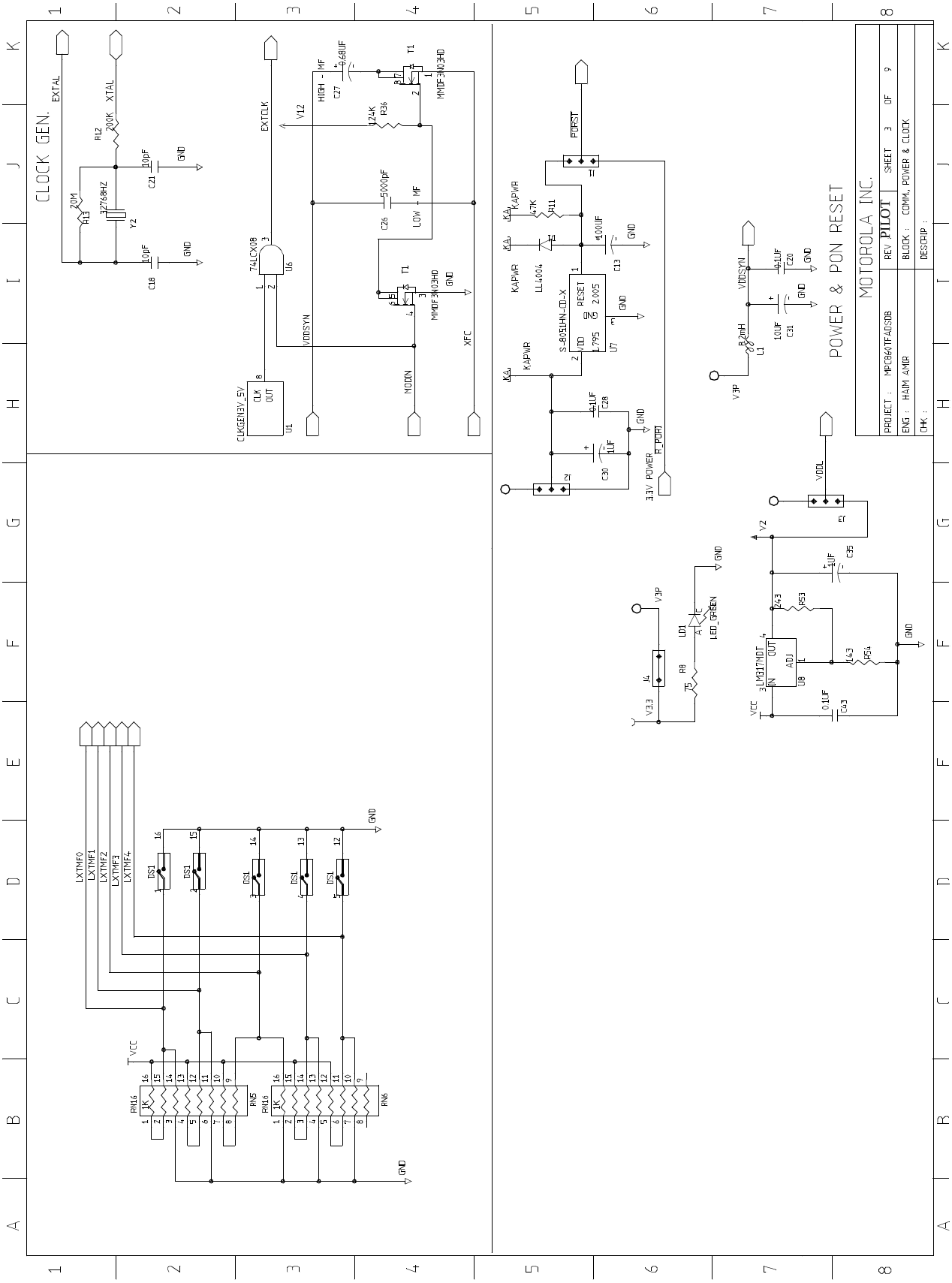
TABLE 5-18. PILOT Part List

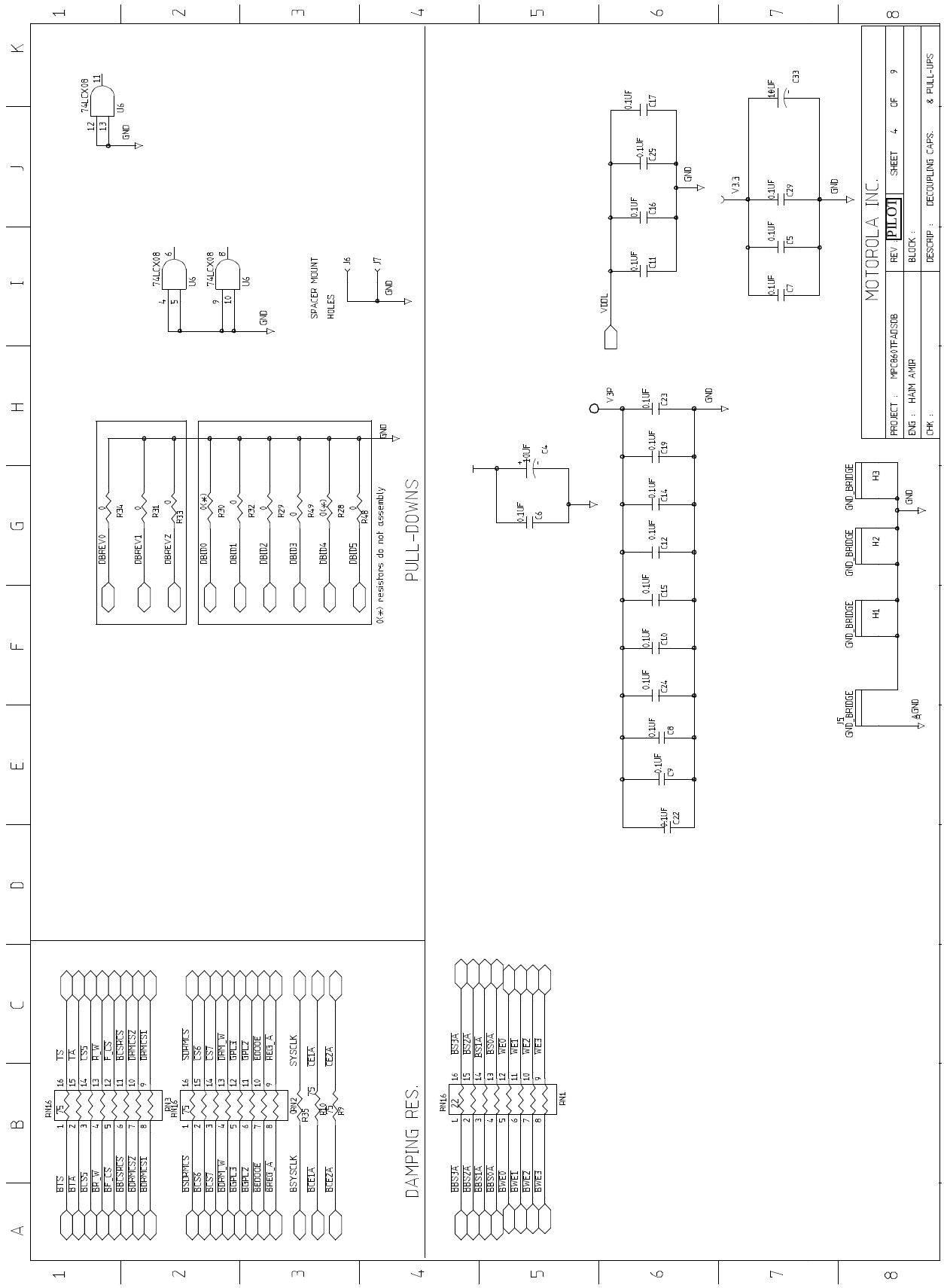
Reference Designation	*Part Description*	*Type*	*Part Number*	total
RN1 RN2 RN3	Resistor Network 75 Ω, 5%, 8 resistors, 16 pin.	SMD	051 00060	3
RN5 RN6	Resistor Network 1KΩ, 5%, 8 resistors, 16 pin.	SMD	051 00066	2
RN4	Resistor Network 4.7K, 5%, 8 resistors, 14 pin.	SMD	051 00036	1
T1S	MMDF3N03HD Transistor TMOS, Dual, 3A	SMD	051 MMDF3N03HD	1
U1	4 MHz Clock generator. 3.3V, CMOS levels.	TH	048 00072	1
U1 Socket	14 pin PC Socket	TH	009 00135	1
U2	MPC860T, 19 X 19, 357 pin BGA. MPC860 or MPC860SAR or MPC860T	TH	009 00284	1
U2 Socket	361 pin 19 X 19 BGA ZIF Socket	TH	009 00284	1
U3	OPTICAL TRANCEIVER This device is not mounted on the board. if the user wants to use fiber optic he should populate it.	TH		1
U4	LXT970 F-ETHERNET TRANCEIVER	TH	051 LXT970QC	1
U5	TG-223506 LAN Magnetics	TH	091 TG-223506ND	1
U6	74LCX08D Quad Low Voltage CMOS AND Gate.	SMD	051 74LCX08D	1
U7	S-8051HN-CD-X Voltage level detector. Range 1.795V to 2.005V. O.D. output.	SMD	051 S-8051	1
U8	LM317MDT Variable Output Voltage regulator.	SMD	051 LM317MD	1
Y1	CTX093 25Mhz CRYSTAL	TH	048 00099	1
Y2	Crystal resonator, 32.768 KHz, Frequency tolerance ± 30 ppm, Drive-level - 10µW Max, Shunt capacitance - 2pF Max., Load capacitance - 12.5pF Max., Equivalent Series Resistance - 35 KΩ Max.	SMD	048 00034	1

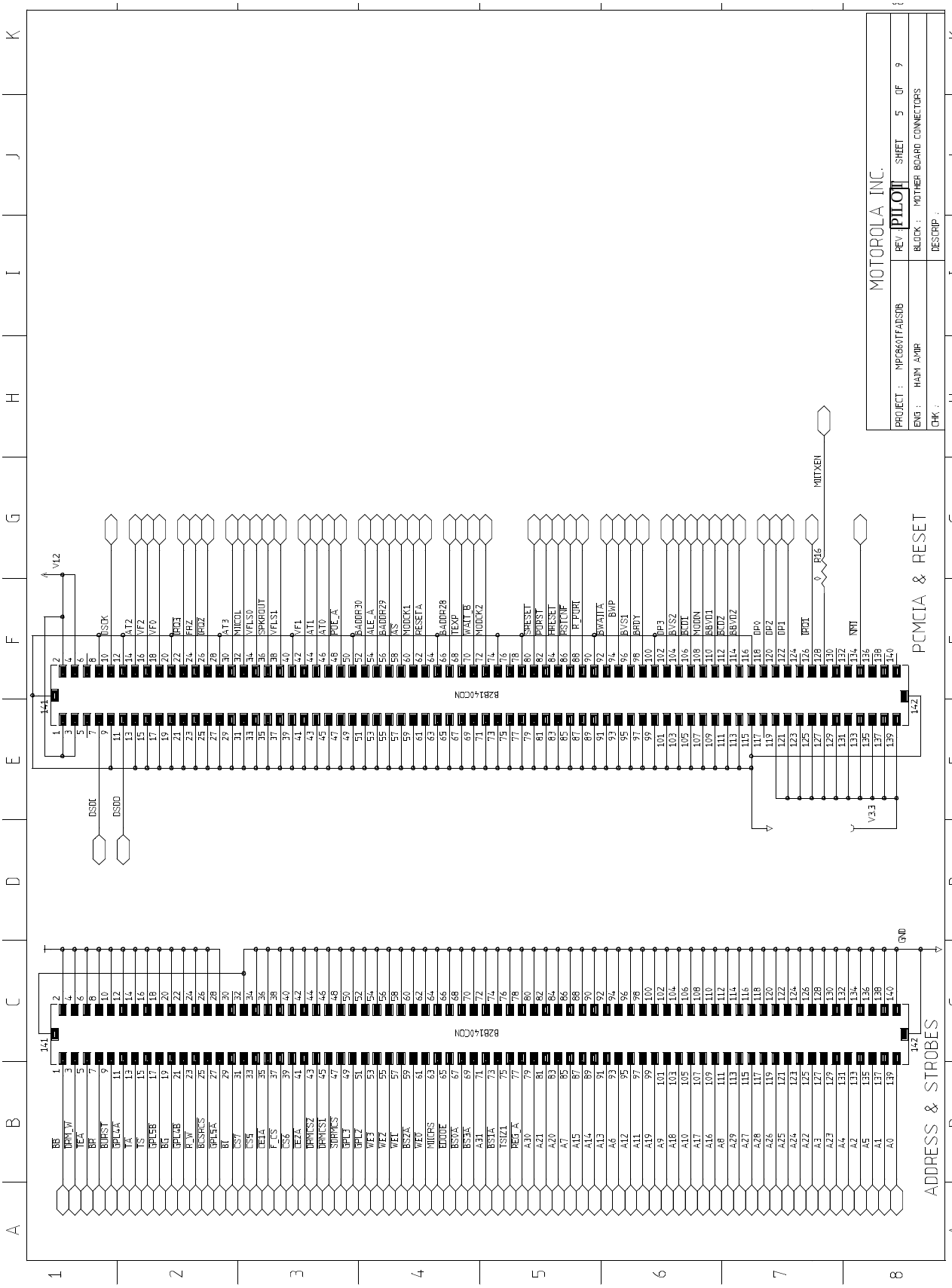
Support Information

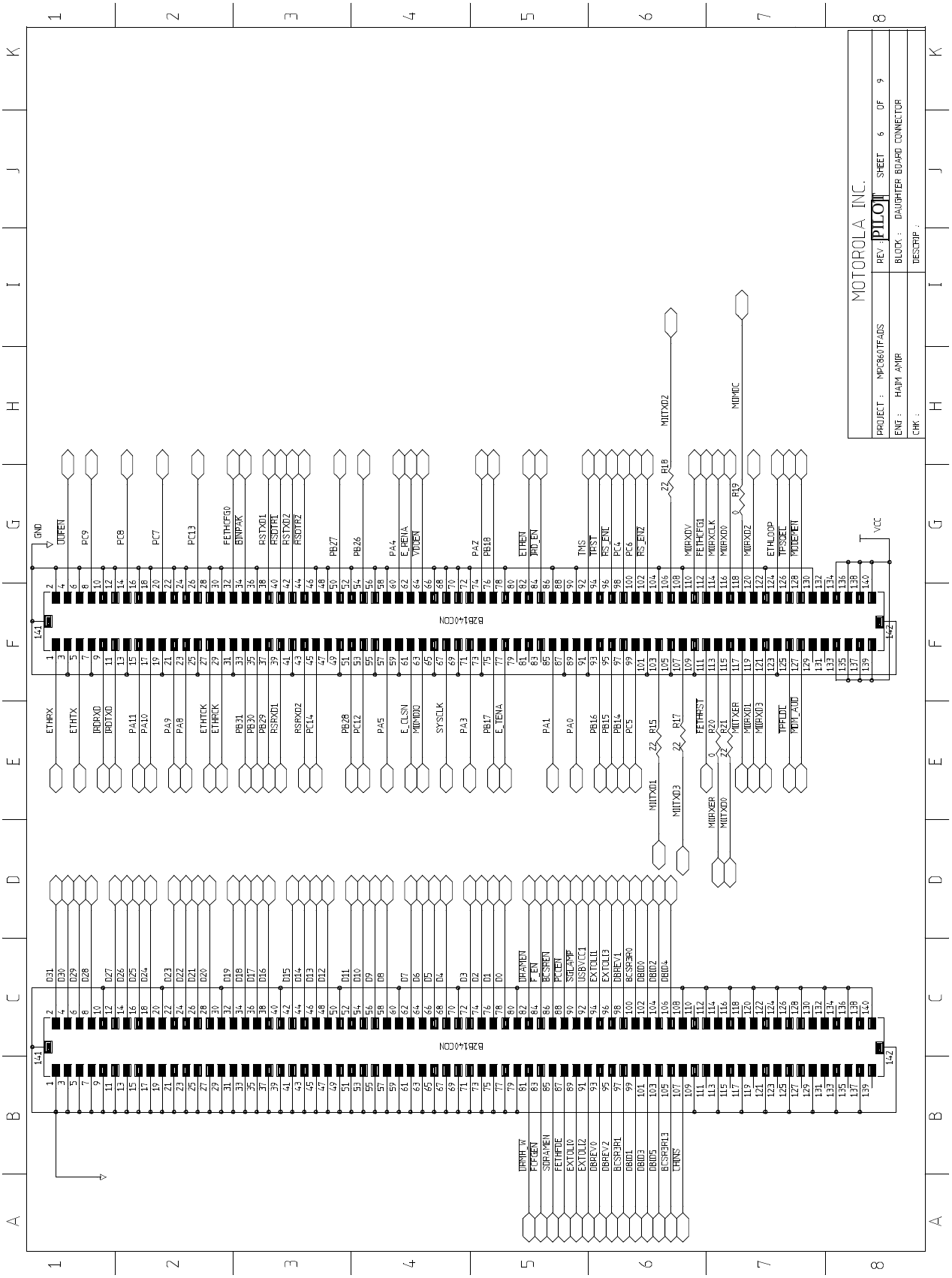


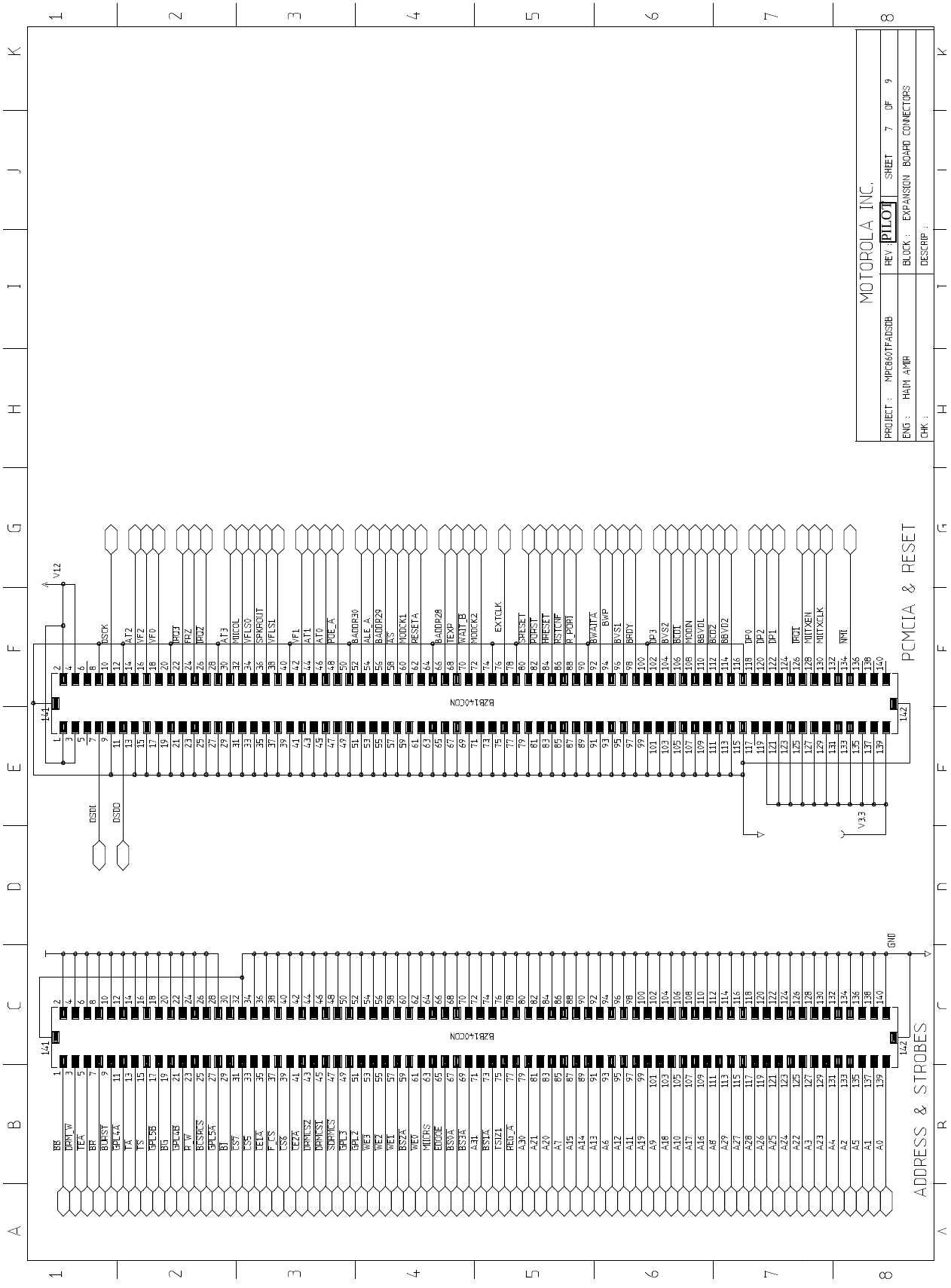

MOTOROLA INC.
PROJECT : MPC860TF-ADSDB
ENG : HAM ANDR
REV : PILOT
BLOCK : FAST ETHERNET TRANCEIVER
SHEET 2 OF 9
DESCRIP :
CHK :
HALO
LXT970
SC_CONNECTOR
HFBR-5205
HFBR-5103 or HFBR-5105 OPTIONAL
RJ_45_8
LED_GREEN
25MHz
10K
4.7K

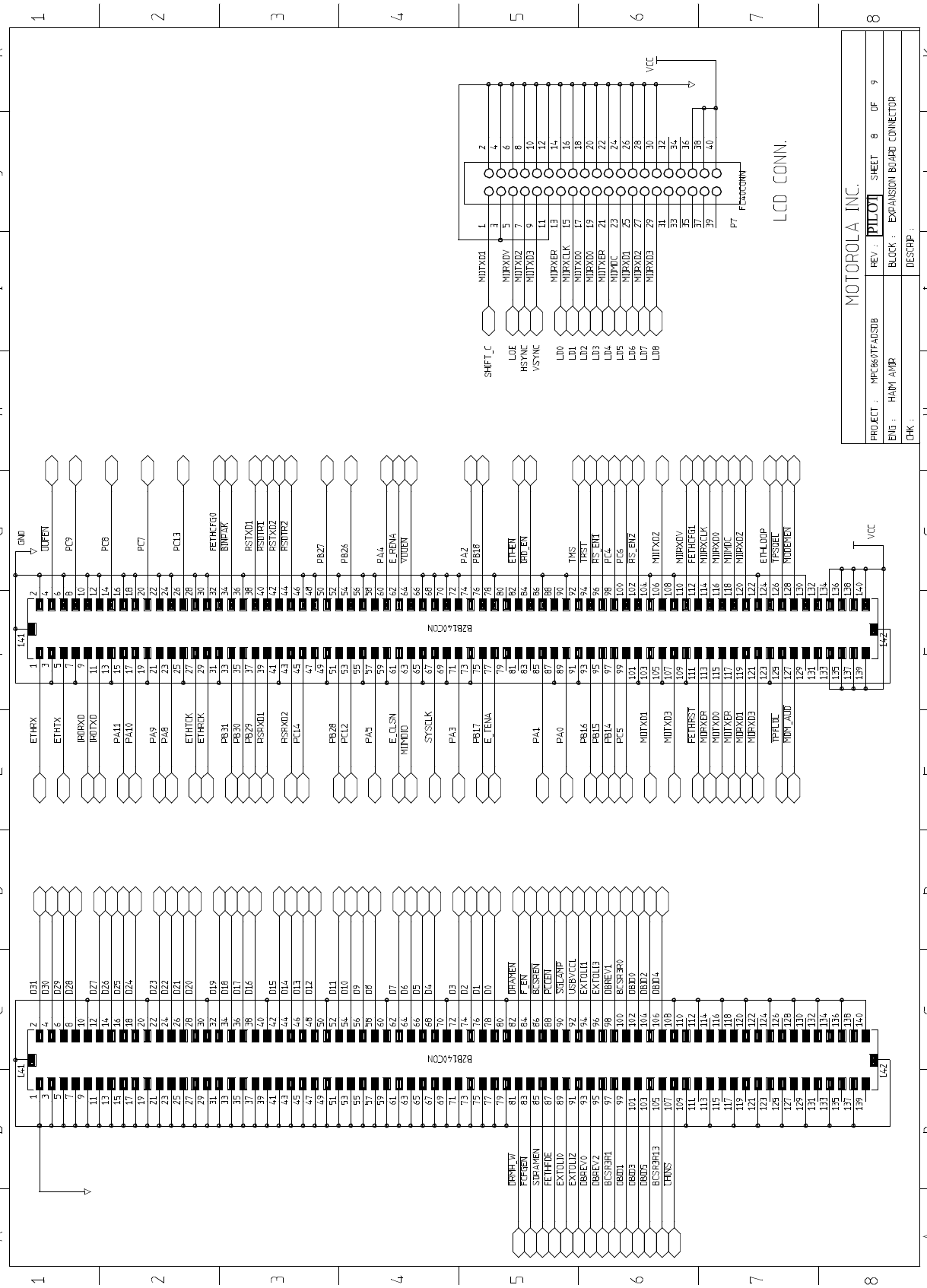

CLOCK GEN.
EXTAL
XTAL
R12
200K
20M
R13
32.768KHZ
Y2
C21
10pF
C18
10pF
GND
EXTCLK
V12
74LCX08
U16
CLKGEN3V_5V
U1
CLK
OUT
HIGH - MF
C27
0.68UF
T1
MMDF3N03HD
124K
R36
5600pF
C26
LOW - MF
VDDSYN
MODIN
XFC
POR
KAPWR
4.7K
R11
LL4004
S-8051HN-TD-X
RESET
2.90V
U7
VTD
1.79V
C28
0.1UF
C30
1UF
3.3V POWER
P_POR1
J7
J1
410UF
C13
MOTOROLA INC.
PROJECT : MPC860TF-ADSDB
REV PILOT
SHEET 3 OF 9
ENG : HARM AMIR
BLOCK : COMM, POWER & CLOCK
CHK :
DESCRIP :
POWER & PON RESET
V3P
8.2nH
L1
10UF
C31
0.1UF
C20
V2
J2
VDDL
C35
1UF
R43
R53
R54
LM317MDT
U8
ADJ
VCC
C43
0.1UF
LD1
LED_GREEN
R8
75
J4
V3.3
LXTMF0
LXTMF1
LXTMF2
LXTMF3
LXTMF4
DS1
RN16
RN5
RN6
1K

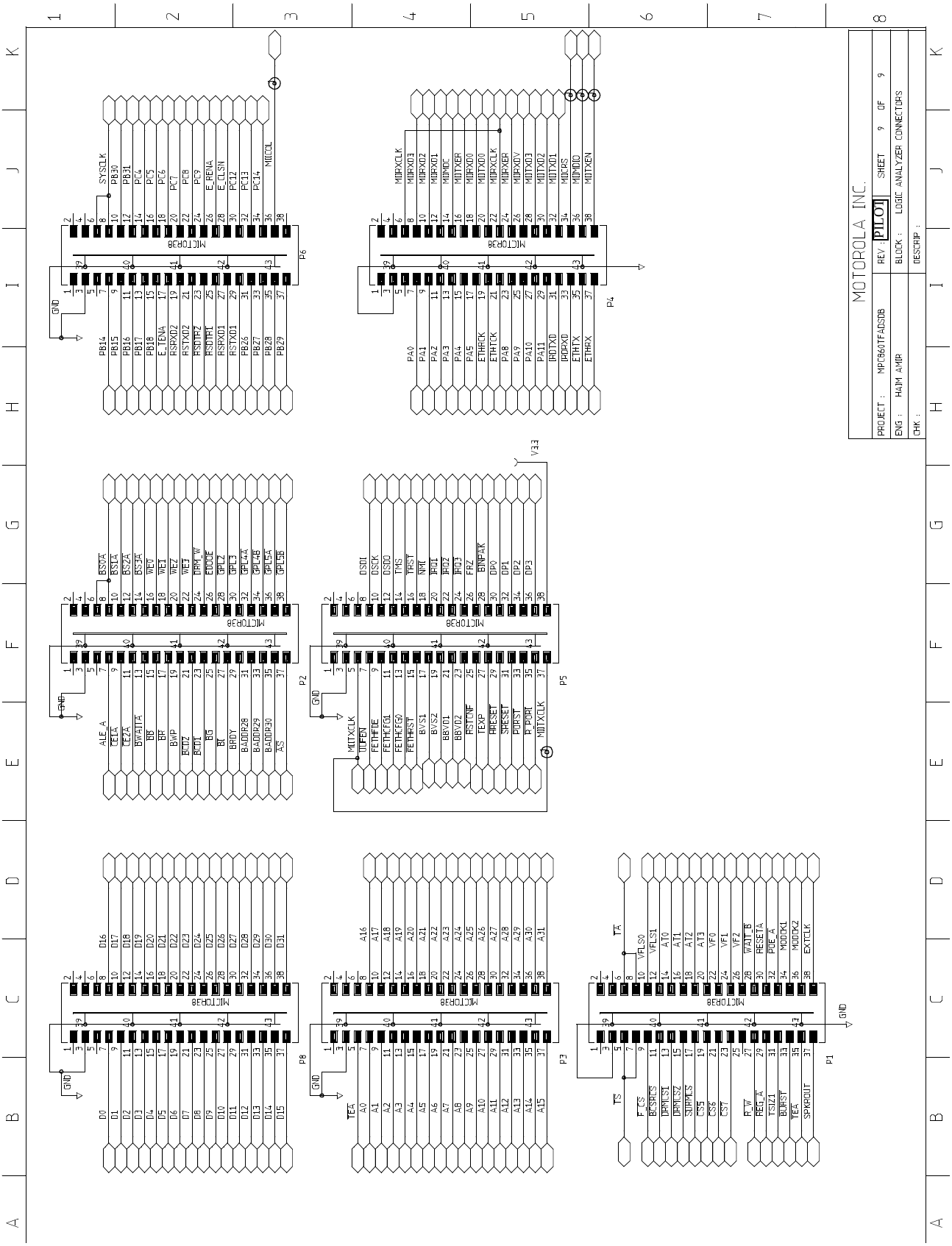

PULL-DOWNS
DAMPING RES.
MOTOROLA INC.
PROJECT : MPC860TP-ADSDB
ENG : HAJM &MP
CHK :
REV : PILOT
BLOCK :
DESCRIP : DECOUPLING CAPS. & PULL-UPS
SHEET 4 OF 9
0(*) resistors do not assembly
SPACER MOUNT HOLES
GND_BRIDGE
VDDL
V3P
V3.3
GND
AGND


MOTOROLA INC.
PROJECT : MPC860TFADSDB
ENG : HAIM AMIR
CHK :
REV : PILOT
SHEET 5 OF 9
BLOCK : MOTHER BOARD CONNECTORS
DESCRIP :
PCMCIA & RESET
ADDRESS & STROBES
B2814OCON
MDTXEN
R16
V12
V3.3
GND
DSDI
DSDO
DSCK




MOTOROLA INC.
PROJECT : MPC860TFADSDB
REV : PILOT
SHEET 7 OF 9
ENG : HAIM AMIR
BLOCK : EXPANSION BOARD CONNECTORS
CHK :
DESCRIP :
PCMCIA & RESET
ADDRESS & STROBES
B2B140CON
V12
V33
GND
DSDI
DSDO


LCD CONN.
MOTOROLA INC.
PROJECT : MPC860TFADSDB
ENG : HADM AMPP
CHK :
REV : PILOT1
BLOCK : EXPANSION BOARD CONNECTOR
DESCRIP :
SHEET 8 OF 9
P7
FLEXCONN
VCC
GND
B2814CON
L41
L42


MOTOROLA INC.
PROJECT : MPC860TFADSDB
REV : [PILOT]
SHEET 9 OF 9
ENG : HAJM AMIR
BLOCK : LOGIC ANALYZER CONNECTORS
CHK :
DESCRIP :
P6
P4
P2
P5
P8
P3
P1
MICTOR38

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